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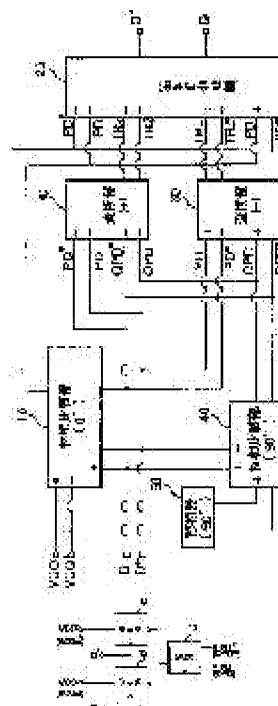
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## (54) PHASE FREQUENCY COMPARATOR

### (57)Abstract:

**PURPOSE:** To provide a circuit easy to use in an integrated circuit comprised of a GaAsMESFET and to reduce the high frequency component of output by constituting the circuit of first and second phase comparison parts, a conversion part, and a registration part, and using a pair of latches and a pair of multiplexers in the phase comparison parts.

**CONSTITUTION:** Voltage controlled oscillator output VCO, VCO\* are inputted to the latches 11, 12, and data signals D, D\* to the control terminals of the latches 11, 12. The signal D is also inputted to the control terminal of a MUX 13. The MUX 13 outputs phase comparison output PD, PD\* (QPD, QPD\*) to the conversion parts 30, 60. The conversion parts 30, 60 output signals TR, TR\*. The signal TR is a pulse synchronized with the output PD and the signal TR\* is the one synchronized with the output PD\* when it is  $f_{vco} < f_D$ , and signals TR+\* and TR-\* go to H. The signal TR+\* is a pulse synchronized with the output PD\* and the signal TR-\* is the one synchronized with the output PD when it is  $f_{vco} > f_D$ , and signals TR+, TR- go to H. The registration part 20 outputs output signals Q, Q\* on which a DC bias voltage Vo is added by receiving the output signals TR+, TR+\*, TR-, TR-\*, and signals PD, PDP.



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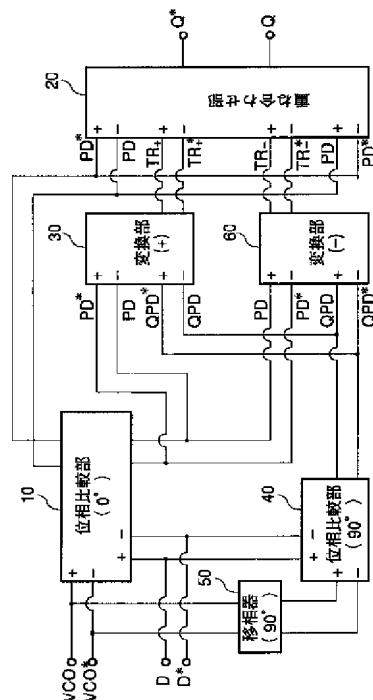
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(54)【発明の名称】 位相周波数比較回路

(57)【要約】

【構成】電圧制御発振器の発生する所定の周波数の参照信号および所定のクロック信号を基準とするデータ信号を受ける第1の位相比較部10と、該参照信号の位相を90度シフトする移相器50と、該移相器50の出力および該データ信号を受ける第2の位相比較部40と、該第1および第2の位相比較部10、40の位相比較出力を周波数比較出力に変換する正相および逆相の変換部30、60と、該位相比較部10の位相比較出力と該変換部30、60の周波数比較出力とを受けてそれらの和を出力する重ね合わせ部20とを備える位相周波数比較回路。



## 【特許請求の範囲】

【請求項1】電圧制御発振器の発生する所定の周波数の参照信号および所定のクロック信号を基準とするデータ信号を受ける第1の位相比較部と、該参照信号の位相を90度シフトする移相器と、該移相器の出力および該データ信号を受ける第2の位相比較部と、該第1および第2の位相比較部の位相比較出力を周波数比較出力に変換する正相および逆相の1対の変換部と、該位相比較部の位相比較出力と該変換部の周波数比較出力とを受けてそれらの和を出力する重ね合わせ部とを備えることを特徴とする位相周波数比較回路。

## 【発明の詳細な説明】

## 【0001】

【産業上の利用分野】本発明は位相周波数比較回路に関する。より詳細には、本発明は、GaAsMESFET集積回路として形成することができる新規な位相周波数比較回路の構成に関する。

## 【0002】

【従来の技術】図9は、従来の位相周波数比較回路の典型的な構成を示す図である。

【0003】同図に示すように、この位相周波数比較回路は、3つのJ-Kフリップフロップ91、92、93により構成されており、J端子入力の“OR”をとったパルスの立ち上がりで $Q_2$ 端子、 $Q_3$ 端子を“1”にし、K端子入力のORで $Q_1^*$ 端子、 $Q_2^*$ 端子を“0”にする構成となっている。

## 【0004】

【発明が解決しようとする課題】上述のような従来の位相周波数比較回路を使用した場合、例えばクロックデータ再生回路を構成するためには、NRZデータ列からクロック成分を抽出する回路が必要になる。また、位相周波数比較出力をチャージポンプ回路を介してループフィルタに入力する必要がある。しかしながら、近年利用の拡大しているGaAsMESFETによる集積回路ではチャージポンプ回路を構成することが困難であることが知られている。

【0005】そこで、本発明は、上記従来技術の問題点を解決し、GaAsMESFETによる集積回路においても有効に使用することができる新規な位相周波数比較回路を提供することをその目的としている。

## 【0006】

【課題を解決するための手段】本発明に従うと、電圧制御発振器の発生する所定の周波数の参照信号および所定のクロック信号を基準とするデータ信号を受ける第1の位相比較部と、該参照信号の位相を90度シフトする移相器と、該移相器の出力および該データ信号を受ける第2の位相比較部と、該第1および第2の位相比較部の位相比較出力を周波数比較出力に変換する正相および逆相の1対の変換部と、該位相比較部の位相比較出力と該1対の変換部の周波数比較出力とを受けてそれらの和を出力

する重ね合わせ部とを備えることを特徴とする位相周波数比較回路が提供される。

## 【0007】

【作用】本発明に係る位相周波数比較回路は、特に、GaAsMESFET集積回路において利用し易く構成されていることと、その出力に含まれる高周波成分が少ないことに主要な特徴がある。

【0008】図1は、本発明に係る位相周波数比較回路の基本的な構成を示す図である。

【0009】同図に示すように、この回路は、第1の位相比較部10、重ね合わせ部20、1対の変換部30、60、第2の位相比較部40および90度移相器50から主に構成されている。尚、図中でこの回路に入力されるVCO、VCO\*は電圧制御発振器の相補的な出力を表し、D、D\*は相補的な入力データ信号を表している。また、位相同期しているときは、VCOおよびVCO\*の周波数 $f_{VCO}$ とデータ信号の基準クロック周波数 $f_D$ とは一致している。

【0010】位相比較部10は、電圧制御発振器出力VCO、VCO\*（周波数 $f_{VCO}$ ）およびデータ信号D、D\*（データレート $f_D$ ）をそのまま受ける。また、位相比較部40は、データ信号D、D\*と共に移相器50により移相が90度シフトされたVCO、VCO\*を受ける。ここで、周波数 $f_{VCO}$ と周波数 $f_D$ とが一致していないとき、位相比較部10、40は周波数 $|f_{VCO} - f_D|$ のビート信号を発生する。また、両者が一致したときには位相のずれに対応した出力が発生する。

【0011】図2は、図1に示した回路において位相比較部10または40として使用できる回路の構成例および動作を説明するための図である。尚、以下の説明において、括弧で囲まれた符号は位相比較部40における信号を、囲まれていない符号は位相比較部10における信号をそれぞれ意味している。

【0012】図2(a)に示すように、この位相比較部は1対のラッチ11、12およびマルチプレクサ13により構成できる。電圧制御発振器出力VCO、VCO\*（VCO<sub>90</sub>、VCO<sub>90</sub>\*）はラッチ11、12の入力に接続されており、データ信号D、D\*はラッチ11、12の制御端子に入力されている。また、ここでは、マルチプレクサ13の制御端子にもデータ信号Dが入力されている。各ラッチ11、12の出力は共にマルチプレクサ13の入力に接続されており、このマルチプレクサ13の出力が位相比較出力PD、PD\*（QPD、QPD\*）となる。

【0013】以上のように構成された位相比較部に入力されるVCO（VCO\*）およびD（D\*）は図2(b)に示すような関係にある。従って、位相比較部の出力は、VCO周波数 $f_{VCO}$ とDの周波数 $f_D$ との関係に応じて下記のように変化する。

【0014】(1)  $f_{VCO}$ が $f_D$ よりも小さいとき；PDは周波数 $(f_D - f_{VCO})$ のパルスである。また、QP

Dは、PDよりも位相が90度進んだ、周波数( $f_D - f_{VCO}$ )のパルスである。

(2)  $f_{VCO}$  が  $f_D$  よりも大きいとき；PDは周波数( $f_{VCO} - f_D$ )のパルスである。また、QPDは、PDよりも位相が90度遅れた、周波数( $f_{VCO} - f_D$ )のパルスである。

(3)  $f_{VCO}$  と  $f_D$  とが等しく、VCOの方がDよりも位相が遅れているとき；PDは“H”レベルに、QPDは“H”レベルになる。

(4)  $f_{VCO}$  と  $f_D$  とが等しく、Dの方がVCOよりも位相が遅れているとき；PDは“L”レベルに、QPDは“H”レベルになる。

【0015】図3は、図1に示した回路において変換部30または60として使用できる回路の基本構成および動作を説明するための図であり、この図では変換部30に相当するものを示している。

【0016】同図に示すように、変換部は、1対のラッチ31、32と1対のNAND33、34により構成することができる。ここで、各ラッチ31、32の入力には、位相比較部10、40の出力であるPD、PD\*、QPD、QPD\*が入力されている。また、各ラッチ31、32の制御端子には、位相比較部10の出力であるPDまたはPD\*が入力されている。更に、ラッチ31の出力は、PD\*と共にNAND33に入力される。また、ラッチ32の出力はPDと共にNAND34に入力される。NAND33、34の出力がこの変換部の出力TR<sub>+</sub>、TR<sub>+</sub>\*となる。

【0017】尚、変換部60は、基本的には同じ構成を有しているが、PD、PD\*、QPD、QPD\*の各信号を受けてTR<sub>-</sub>、TR<sub>-</sub>\*を出力する。

【0018】以上のように構成された変換部30、60の出力は、電圧制御発振器出力VCOの周波数 $f_{VCO}$ とデータ信号Dの周波数 $f_D$ との関係に応じて下記のように変化する。

【0019】(1)  $f_{VCO}$  が  $f_D$  よりも小さいとき；TR<sub>+</sub>はPDと、TR<sub>-</sub>はPD\*とそれぞれ同期したパルスであり、TR<sub>+</sub>\*およびTR<sub>-</sub>\*は、“H”レベルになる。

(2)  $f_{VCO}$  が  $f_D$  よりも大きいとき；TR<sub>+</sub>\*はPD\*は、TR<sub>-</sub>\*はPDとそれぞれ同期したパルスであり、TR<sub>+</sub>、TR<sub>-</sub>は“H”レベルになる。

(3)  $f_{VCO}$  と  $f_D$  とが等しく、VCOの方がDよりも位

相が遅れているとき；( $f_{VCO} < f_D$ の状態から $f_{VCO} = f_D$ に近づいたとき)TR<sub>+</sub>、TR<sub>+</sub>\*およびTR<sub>-</sub>\*は共に“H”レベルになり、TR<sub>-</sub>は“L”レベルになる。

(4)  $f_{VCO}$  と  $f_D$  とが等しく、Dの方がVCOよりも位相が遅れているとき；( $f_{VCO} > f_D$ の状態から $f_{VCO} = f_D$ に近づいたとき)TR<sub>+</sub>、TR<sub>+</sub>\*およびTR<sub>-</sub>は共に“H”レベルになり、TR<sub>-</sub>\*は“L”レベルになる。

【0020】図4は、図1に示した回路において重ね合わせ部20として使用できる回路の構成および動作を説明するための図である。

【0021】同図に示すように、この回路は、各々1対の相補的な入力および出力を有する3つの差動増幅器21、22、23により構成された1対の単位重ね合わせ部X、Yを組み合わせる構成されている。即ち、各单位重ね合わせ部X、Yでは、差動増幅器21、23の反転入力とは所定の参照電圧V<sub>ref</sub>を共通に受けている。また、差動増幅器21および23の非反転入力、変換部30の出力TR<sub>+</sub>、TR<sub>+</sub>\*または変換部60の出力TR<sub>-</sub>、TR<sub>-</sub>\*を受けている。更に、差動増幅器22の入力は、位相比較部10の相補的な出力PD\*、PDを受けている。一方、差動増幅器22の反転出力は、差動増幅器21の反転出力と加算された後、更に差動増幅器23の非反転出力と加算される。また、差動増幅器22の非反転出力は、差動増幅器23の反転出力と加算された後、更に差動増幅器21の非反転出力と加算される。このような単位重ね合わせ部X、Yの出力は、更に互いに加算されて、この重ね合わせ部の出力Q、Q\*として出力される。尚、実際には、各出力Q、Q\*には、直流バイアス電圧V<sub>0</sub>が更に加算されて出力される。

【0022】以上のように構成された重ね合わせ部の出力Q、Q\*は、周波数 $f_{VCO}$ と周波数 $f_D$ との関係により変化する。図5は、周波数 $f_{VCO}$ と周波数 $f_D$ との関係により変化するこの回路の出力Q、Q\*を示す図である。

【0023】表1に、各状態における各増幅器21、22、23の出力レベルを示す。

【0024】

【表1】

| 出力レベル    | “H”レベル            | “L”レベル              |
|----------|-------------------|---------------------|
| 増幅器21、23 | V <sub>0f</sub>   | - V <sub>0f</sub>   |
| 増幅器22    | 2 V <sub>0f</sub> | - 2 V <sub>0f</sub> |

【0025】(1)  $f_{VCO}$  が  $f_D$  よりも小さいとき(図5(a)に示す)； $Q = V_0 - V_{of}$ 、 $Q^* = V_0 + V_{of}$

(2)  $f_{VCO}$  が  $f_D$  よりも大きいとき(図5(a)に示

す)； $Q = V_0 + V_{of}$ 、 $Q^* = V_0 - V_{of}$

(3)  $f_{VCO}$  と  $f_D$  とが等しく、VCOの方がDよりも位相が遅れているとき；( $f_{VCO} < f_D$ の状態から $f_{VCO}$

$= f_D$  に近づいたとき、図5(c)に示す)  $Q = V_0 - V_{of}$ 、 $Q^* = V_0 + V_{of}$

(4)  $f_{VCO}$  と  $f_D$  とが等しく、Dの方がVCOよりも位相が遅れているとき；( $f_{VCO} > f_D$  の状態から  $f_{VCO} = f_D$  に近づいたとき、図5(d)に示す)  $Q = V_0 + V_{of}$ 、 $Q^* = V_0 - V_{of}$

【0026】以上のように構成された本発明に係る位相周波数比較回路は、その直後にループフィルタを追加することにより、電圧制御発振器の位相および周波数が一致するような位相同期制御を行うための制御信号を発生することができる。

【0027】また、この方式では、データ信号からクロック成分を抽出するための回路や、チャージポンプ回路等を付加することなく所期の機能を実現することができる。従って、チャージポンプ回路を構成することが困難なGaAsMESFET集積回路においても使用することができる。

【0028】更に、図5からも判るように、この位相周波数比較器の構成においては、非同期時からの周波数引込み過程においてビート信号等に起因する高周波成分が一切出力されない。従って、出力信号の高周波成分に起因する移相同期ループの誤動作が生じる恐れがない。また、図5(c)に示すようにこの位相周波数比較回路は理想的な出力波形を有しており、これに接続する位相同期ループの設計は容易である。

【0029】尚、本発明の一態様に従うと、図1に示した位相周波数比較回路において、位相比較部10、40をD型フリップフロップにより構成することもできる。図10は、D型フリップフロップを使用して構成する位相比較部の機能を説明するための図である。

【0030】図10(a)に示すように、D型フリップフロップに対して、電圧制御発振器の出力VCO、VCO\*をデータ入力に投入し、データの基準クロック信号をD型フリップフロップの制御入力に投入する。ここで、D型フリップフロップに投入されるVCO(VCO\*)およびクロック信号CK(CK\*)は、図10(b)に示すような関係にある。従って、位相比較部の出力DFFは、VCOの周波数 $f_{VCO}$ およびクロック信号CKの周波数 $f_{CK}$ により以下のように変化する。

【0031】(1)  $f_{VCO}$  が  $f_{CK}$  よりも小さいとき；DFFは周波数( $f_{CK} - f_{VCO}$ )のパルスである。また、QDFFは、DFFよりも位相が90度進んだ、周波数( $f_{CK} - f_{VCO}$ )のパルスである。

(2)  $f_{VCO}$  が  $f_{CK}$  よりも大きいとき；DFFは周波数( $f_{VCO} - f_{CK}$ )のパルスである。また、QDFFは、DFFよりも位相が90度遅れた、周波数( $f_{VCO} - f_{CK}$ )のパルスである。

(3)  $f_{VCO}$  と  $f_{CK}$  とが等しく、VCOの方がDよりも位相が遅れているとき；DFFは“H”レベルに、QDFFは“L”レベルになる。

(4)  $f_{VCO}$  と  $f_{CK}$  とが等しく、Dの方がVCOよりも位相が遅れているとき；DFFは“L”レベルに、QDFFは“L”レベルになる。

【0032】従って、図1に示した位相周波数比較回路の位相比較部10、40としてD型フリップフロップを用い、位相比較部10、40の出力PD、PD\*、QPD、QPD\*に代わって、D型フリップフロップの出力DFF、DFF\*、QDFF、QDFF\*を用いることにより、この位相周波数比較部は図1に示した構成について既に説明した場合と同様に動作する。但し、この構成では、D型フリップフロップに供給するためのクロック信号CKが必要になる。

【0033】以下、実施例を参照して本発明を具体的に説明するが、以下の開示は本発明の一実施例に過ぎず、本発明の技術的範囲を何ら限定するものではない。

【0034】

【実施例】図6は図2に示した位相比較部の、より具体的な構成例を示す図である。

【0035】同図に示すように、この回路の各入力端は、電圧制御発振器の相補な出力VCO、VCO\*をそれぞれゲートに受ける各1対のFET $Q_{11} - Q_{12}$ 、 $Q_{21} - Q_{22}$ と、データ信号D、D\*をゲートに受ける1対のFET $Q_{31} - Q_{32}$ とを備えている。

【0036】また、FET対 $Q_{11} - Q_{12}$ 、 $Q_{21} - Q_{22}$ には、FET $Q_{15}$ 、 $Q_{25}$ を含む電流路をゲートに接続されたFET $Q_{14}$ 、 $Q_{24}$ がFET $Q_{11}$ 、 $Q_{21}$ 側に、FET $Q_{16}$ 、 $Q_{26}$ を含む電流路をゲートに接続されたFET $Q_{13}$ 、 $Q_{23}$ がFET $Q_{12}$ 、 $Q_{22}$ 側にそれぞれ接続されている。

【0037】更に、FET $Q_{15}$ 、 $Q_{25}$ を含む電流路にはFET $Q_{17}$ 、 $Q_{27}$ のゲートが、FET $Q_{16}$ 、 $Q_{26}$ を含む電流路にはFET $Q_{18}$ 、 $Q_{28}$ のゲートがそれぞれ接続されている。FET $Q_{17}$ および $Q_{27}$ の一端はFET $Q_{33}$ のゲートに、FET $Q_{18}$ および $Q_{28}$ の一端はFET $Q_{34}$ のゲートにそれぞれ接続されており、この回路の出力端は、FET $Q_{33}$ 、 $Q_{34}$ とレベルシフトダイオード群とにより構成されている。FET $Q_{19}$ のゲートと $Q_{29}$ のゲートとは相互に接続されている。

【0038】尚、データ信号Dのみは、マルチプレクサの制御信号としてFET $Q_{20}$ 、 $Q_{30}$ のゲートにも印加されている。また、FET対 $Q_{19} - Q_{20}$ 、 $Q_{31} - Q_{32}$ 、 $Q_{29} - Q_{30}$ およびFET $Q_{15}$ 、 $Q_{16}$ 、 $Q_{25}$ 、 $Q_{26}$ 、 $Q_{33}$ 、 $Q_{34}$ は、それぞれFET $Q_{35} \sim Q_{43}$ により構成された電流源を個別に備えている。

【0039】以上のように構成された回路において、電圧制御発振器出力VCO、VCO\*によりFET $Q_{11} - Q_{21}$ 、 $Q_{12} - Q_{22}$ の何れか一方が導通すると、それに応じてFET $Q_{16} - Q_{26}$ 、 $Q_{15} - Q_{25}$ の何れか一方が導通する。更に、FET $Q_{16} - Q_{26}$ 、 $Q_{15} - Q_{25}$ の何れか一方が導通すると、FET $Q_{13} - Q_{18} - Q_{23} - Q_{28}$ 、 $Q_{14}$

$-Q_{17}-Q_{24}-Q_{27}$ の何れか一方が導通する。ここで、各FET対 $Q_{13}-Q_{14}$ 、 $Q_{17}-Q_{18}$ 、 $Q_{21}-Q_{22}$ とFET対 $Q_{11}-Q_{12}$ 、 $Q_{23}-Q_{24}$ 、 $Q_{27}-Q_{28}$ とはデータ信号D、D\*に応じて択一的に有効になるので、FET $Q_{33}$ 、 $Q_{34}$ は択一的に導通する。即ち、電圧制御発振器出力VCO、VCO\*は、データ信号D、D\*によりラッチされ、更に、データ信号D、D\*に応じて出力される。従って出力PD、PD\*には相補的な位相比較出力が得られる。

【0040】図11は、図10に示したD型フリップフロップを用いた場合の位相比較部の具体的な構成例を示す図である。

【0041】同図に示すように、この回路は、互いに同じ構成の回路Aおよび回路Bの2段構成となっており、回路Aの入力は電圧制御発振器出力VCO、VCO\*を、回路Bの入力は回路Aの出力をそれぞれ受けている。回路A(B)の入力端は、入力信号をゲートに受ける1対のFET $Q_{11}-Q_{12}$ ( $Q_{21}-Q_{22}$ )と、クロック信号CK、CK\*をゲートに受ける各1対のFET $Q_{19}-Q_{20}$ ( $Q_{29}-Q_{30}$ )とにより構成されている。尚、FET対 $Q_{19}-Q_{20}$ ( $Q_{29}-Q_{30}$ )およびFET $Q_{15}$ 、 $Q_{16}$ ( $Q_{25}$ 、 $Q_{26}$ )はそれぞれFET $Q_{35}-Q_{37}$ ( $Q_{39}-Q_{41}$ )により構成された電流源を備えている。

【0042】更に、FET $Q_{15}$ ( $Q_{25}$ )を含む電流路にはFET $Q_{14}$ ( $Q_{24}$ )のゲートが、FET $Q_{16}$ ( $Q_{26}$ )を含む電流路にはFET $Q_{13}$ ( $Q_{23}$ )のゲートがそれぞれ接続されている。また、FET $Q_{14}$ ( $Q_{24}$ )の一端はFET $Q_{11}$ ( $Q_{21}$ )の一端に、FET $Q_{13}$ ( $Q_{23}$ )の一端はFET $Q_{12}$ ( $Q_{22}$ )の一端にそれぞれ接続されている。従って、例えばFET $Q_{11}$ ( $Q_{21}$ )が導通するとFET $Q_{16}$ ( $Q_{26}$ )が導通し、このときFET $Q_{13}$ ( $Q_{23}$ )も導通するので、回路A(B)の出力端には相補的な出力が発生する。尚、この回路A(B)の出力端は、ダイオード群を介してFET $Q_{15}$ ( $Q_{25}$ )、 $Q_{16}$ ( $Q_{26}$ )の一端に接続されている。

【0043】以上のように構成された回路は、典型的なD型フリップフロップであり、その機能は図10を参照して既に説明した通りである。従って、本発明に係る回路において、図6に示した位相比較部に代えて使用することができる。

【0044】図7は図1に示した回路における変換部30の具体例を示す図である。

【0045】尚、図3にも示したように、この回路は、位相比較部10の出力PD、PD\*によって、位相比較部40の出力QPD、QPD\*をラッチする1対のラッチ回路と、各ラッチの出力とPD、PD\*とのNANDをとるNANDゲートとから構成されている。従って、図6に比較すると、データ信号D、D\*に代わって位相比較部10の出力PD、PD\*を受け、電圧制御発振器出力VCO、VCO\*に代わって位相比較部40の出力QPD、

QPD\*を受けていることを除いては、ラッチ回路の構成は共通である。一方、図3のNAND回路に相当する、2対のFET $Q_{51}-Q_{52}$ 、 $Q_{53}-Q_{54}$ と出力端とに関連した部分ではこの回路は独自の構成を有している。

【0046】即ち、各FET対 $Q_{51}-Q_{52}$ 、 $Q_{53}-Q_{54}$ は、各ラッチ回路の出力をゲートに受け、位相比較部10の出力PD、PD\*により選択的に有効にされるように構成されている。従って、FET対 $Q_{51}-Q_{52}$ 、 $Q_{53}-Q_{54}$ の出力からは、互いに相補的な変換信号TR、TR\*が出力される。

【0047】図8は重ね合わせ部の具体的な構成例を示す図である。

【0048】同図に示すように、この回路は、各々1対のFET $Q_{61}-Q_{66}$ により構成された3つの差動増幅器21、22、23と、FET $Q_{67}-Q_{69}$ によりそれぞれ構成された電流源部81とからそれぞれが構成された1対の単位重ね合わせ部X、Yを組み合わせて構成されている。

【0049】各单位重ね合わせ部X、Yにおいて、差動増幅器22の一方の出力は、差動増幅器21および23の各一方の出力と結合されており、各差動増幅器21、22、23の他方の出力も相互に結合されている。また、各差動増幅器21、22、23はFET $Q_{67}-Q_{69}$ による電流源81にそれぞれ接続されている。各々がこのような構成を有する単位重ね合わせ部X、Yは、相互に出力を結合されると共に、さらに、抵抗 $R'$ 、 $R_0'$ 、ダイオード群 $D_0'$ およびFET $Q_0'$ により構成された基準電圧発生部Gを共通に接続されている。

【0050】以上のように構成された重ね合わせ部において、単位重ね合わせ部Xにおいては、差動増幅器22の1対の入力であるFET $Q_{64}$ 、 $Q_{63}$ の各ゲートには、位相比較部10の出力信号PD、PD\*が印加される。また、差動増幅器21のFET $Q_{61}$ のゲートおよび差動増幅器23のFET $Q_{66}$ のゲートには、変換部30の出力 $TR_+$ 、 $TR_+^*$ がそれぞれ印加される。更に、差動増幅器21のFET $Q_{62}$ および差動増幅器23のFET $Q_{65}$ のゲートには、基準電圧発生部Gが発生する基準電圧が印加されている。

【0051】一方、単位重ね合わせ部Yにおいては、差動増幅器22の1対の入力であるFET $Q_{64}$ 、 $Q_{63}$ の各ゲートには、位相比較部10の出力信号PD、PD\*が印加される。また、差動増幅器21のFET $Q_{61}$ のゲートおよび差動増幅器23のFET $Q_{66}$ のゲートには変換部60の出力 $TR_-$ 、 $TR_-^*$ がそれぞれ印加される。更に、差動増幅器21のFET $Q_{62}$ および差動増幅器23のFET $Q_{65}$ のゲートには、基準電圧発生部Gが発生する基準電圧が印加されている。

【0052】以上のように構成された回路では、信号PD、PD\*および信号 $TR_+$ 、 $TR_+^*$ の和と、信号PD、PD\*および信号 $TR_-$ 、 $TR_-^*$ の和が更に加算されたものが、信号Q、Q\*として出力される。

【0053】尚、図7および図8に示す回路の基準電圧発生部Gにおいて、図中に示すように、抵抗の抵抗値を $R_0$ 、 $R_1$ 、ダイオードのアノード幅を $D_0$ 、FETのゲート幅を $Q_0$ としたときに、 $Q_0'$ 、 $D_0'$ および $R_1'$ がそれぞれ下記の式1、式2を満足するように作製することにより、簡単な構成で温度変動並びに電源電圧変動に対して安定な基準電圧を発生させることができる。

【0054】

【式1】

$$Q_0' = n Q_0、$$

$$D_0' = n D_0、$$

$$R_1' = (1/n) R_1$$

【0055】

【式2】  $R_0' \cdot I_0' = R_0 \cdot I_0 + R_0 I_1 / 2$

【0056】

【発明の効果】以上説明したように、本発明による位相周波数比較回路は、クロックデータ回路用位相同期ループに対して、データ信号からクロック成分を抽出する回路を別途設ける必要がない。また、ループフィルタとの間にチャージポンプ回路を必要としない。従って、特にチャージポンプを構成し難いGaAsMESFET集積回路において有利に使用することができる。

【0057】更に、本発明に係る位相周波数比較器においては、非同期時からの周波数引込み過程においてビート信号等に起因する高周波成分が一切出力されないの、出力信号の高周波成分に起因する移相同期ループの誤動作が生じる恐れがない。このため、この位相周波数比較回路に接続する位相同期ループの設計が容易になるという効果がある。

【図面の簡単な説明】

【図1】本発明に係る位相周波数比較回路の基本的な構

成を示す図である。

【図2】図1に示した回路において位相比較部10または40として使用できる回路の構成例および動作を説明するための図である。

【図3】図1に示した回路において変換部30として使用できる回路の構成および動作を説明するための図である。

【図4】図1に示した回路において重ね合わせ部20として使用できる回路の構成および動作を説明するための図である。

【図5】図1に示した位相周波数比較回路の出力信号を示す図である。

【図6】位相比較部として使用できる回路の具体的な構成例を示す図である。

【図7】変換部として使用できる回路の具体的な構成例を示す図である。

【図8】重ね合わせとして使用できる回路の具体的な構成例を示す図である。

【図9】従来の位相周波数比較回路の典型的な構成を示す図である。

【図10】D型フリップフロップを使用して構成する位相比較部の機能を説明するための図である。

【図11】図10に示した位相比較部の具体的な構成例を示す図である。

【符号の説明】

10、40・・・位相比較部、

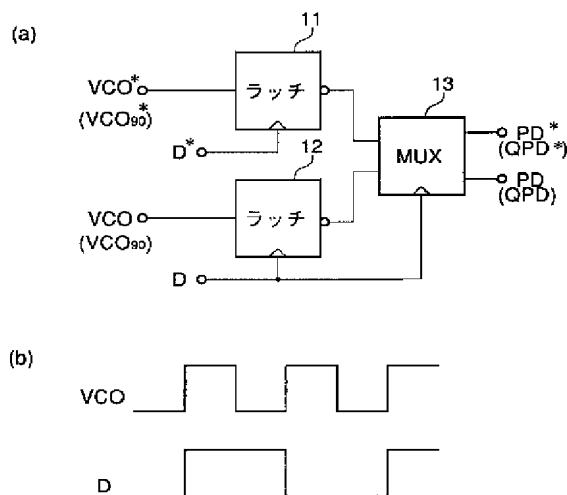
20・・・重ね合わせ部、

30、60・・・変換部、

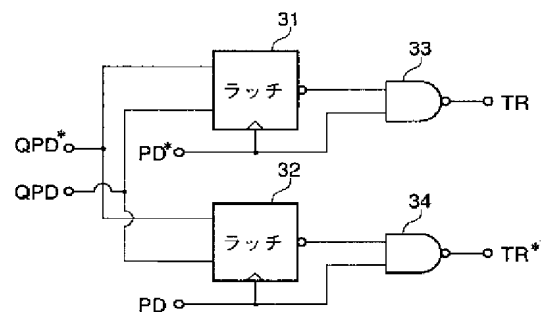
50・・・移相器、

21、22、23・・・差動増幅器

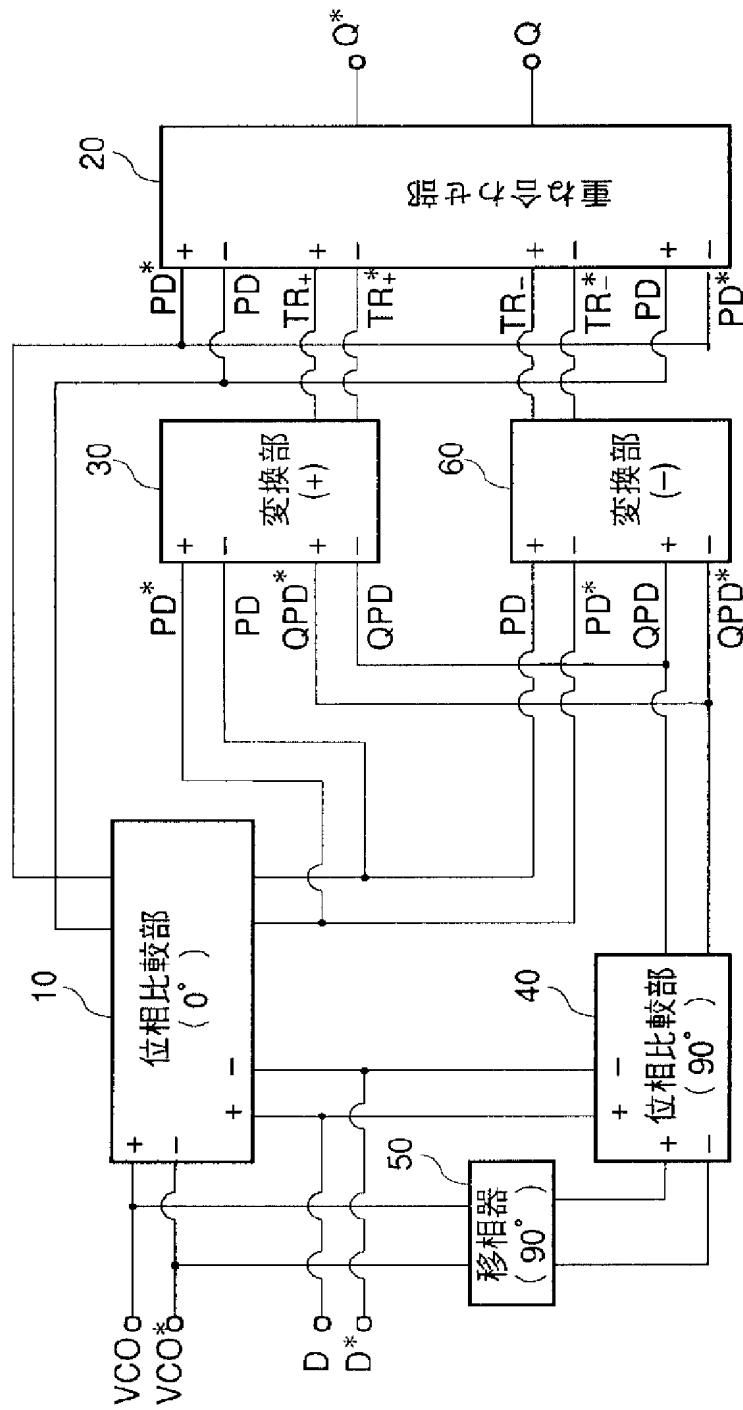
【図2】



【図3】

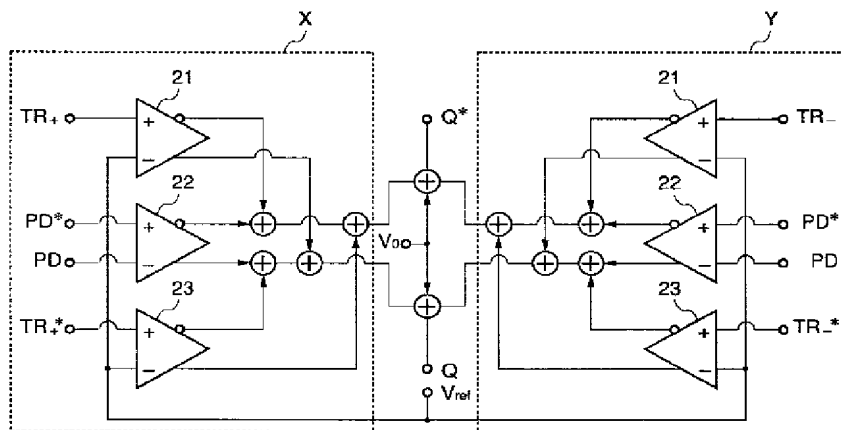


【図1】



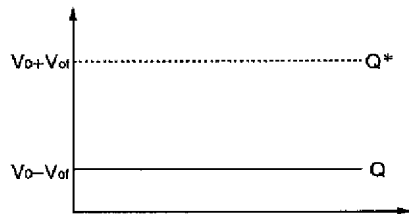


【図4】

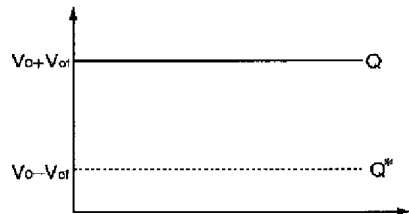


【図5】

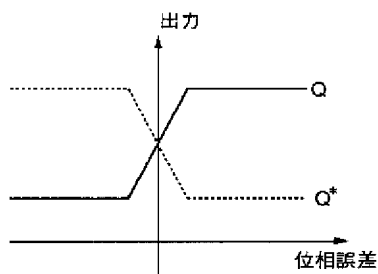
- (a)  $f_{vco} = f_0$ , VCO位相遅れするとき  
( $f_{vco} < f_0$ の状態から近づいたとき)



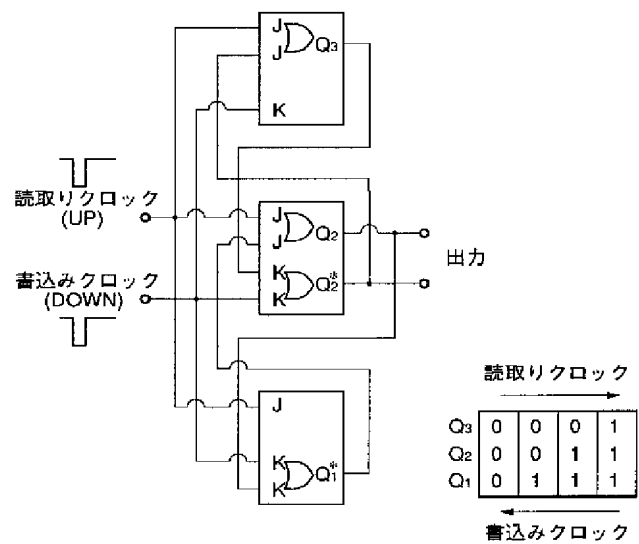
- (b)  $f_{vco} = f_0$ , VCO位相遅れするとき  
( $f_{vco} > f_0$ の状態から近づいたとき)



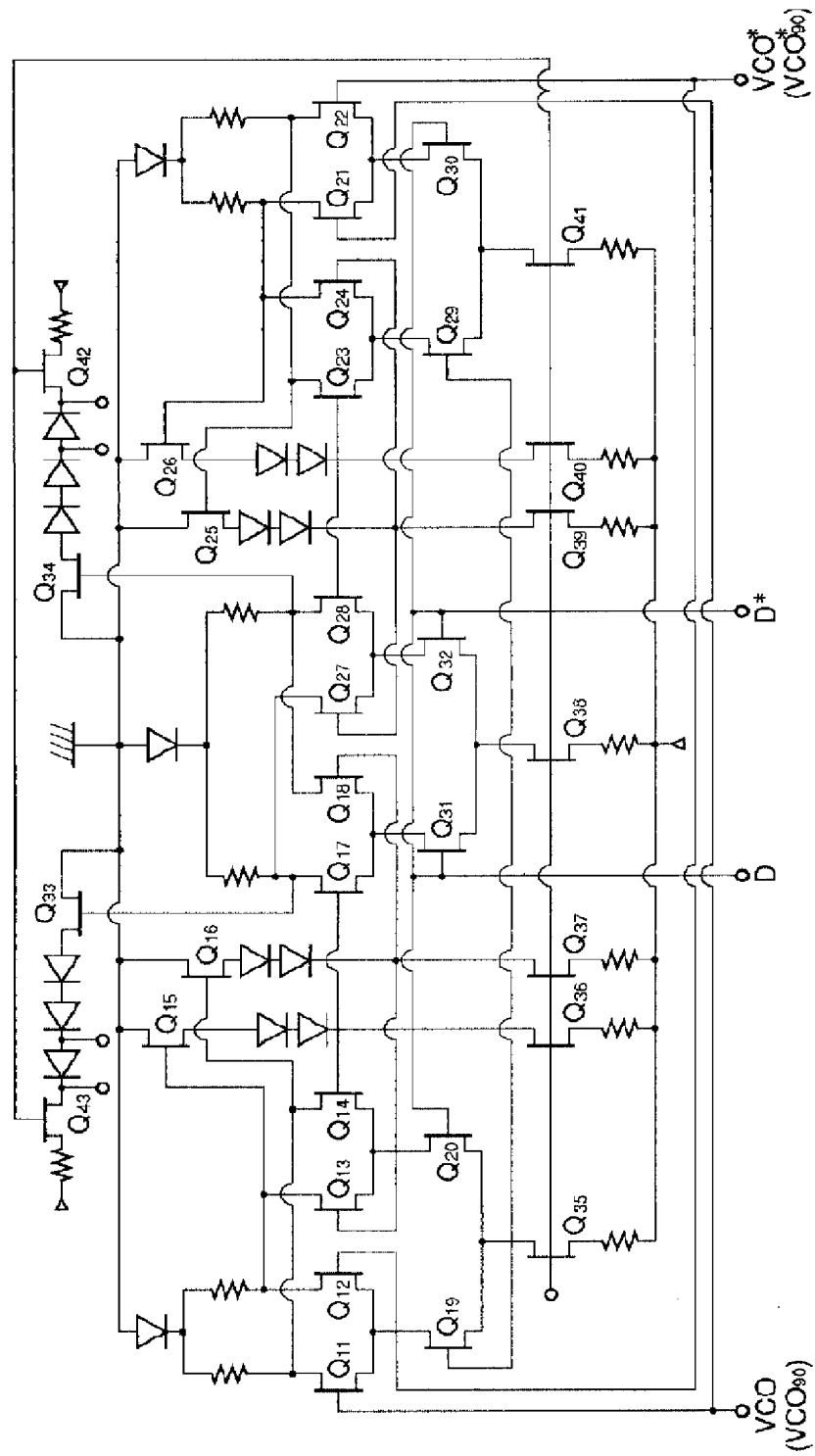
- (c)



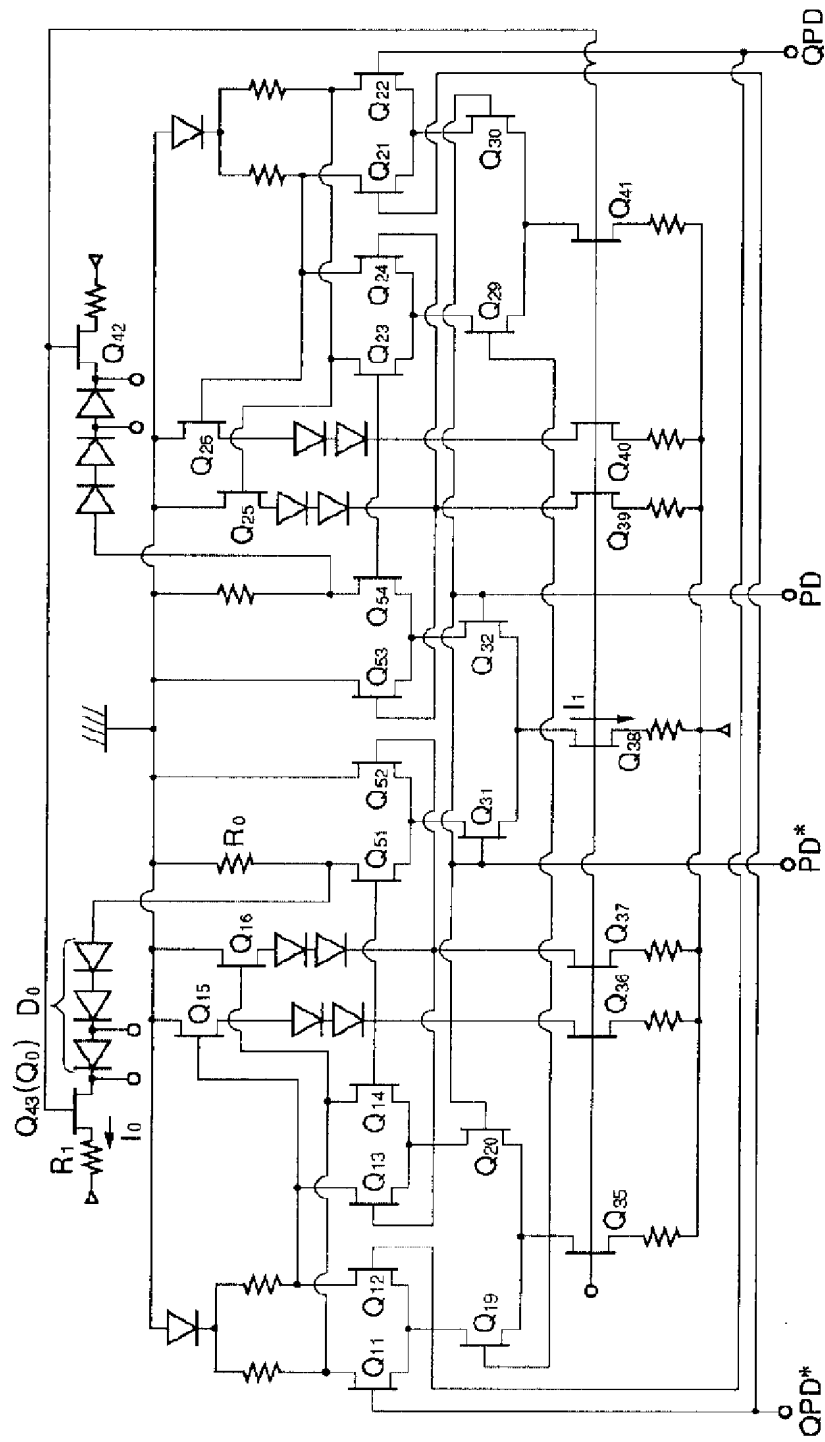
【図9】



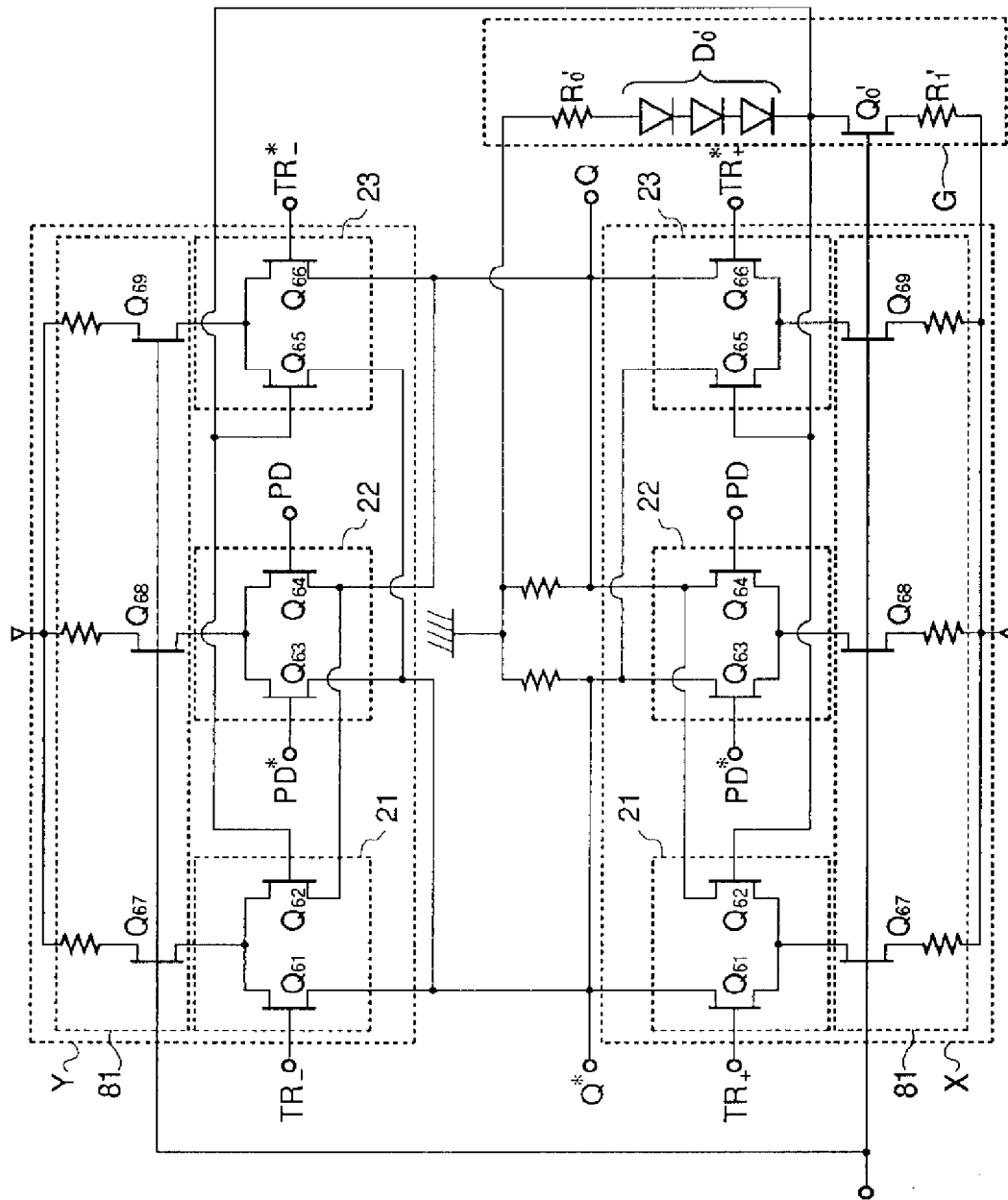
【図6】



【図7】

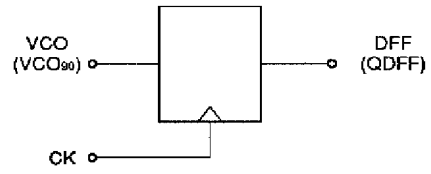


【図8】

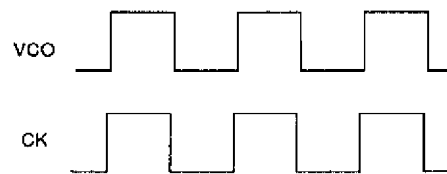


【図10】

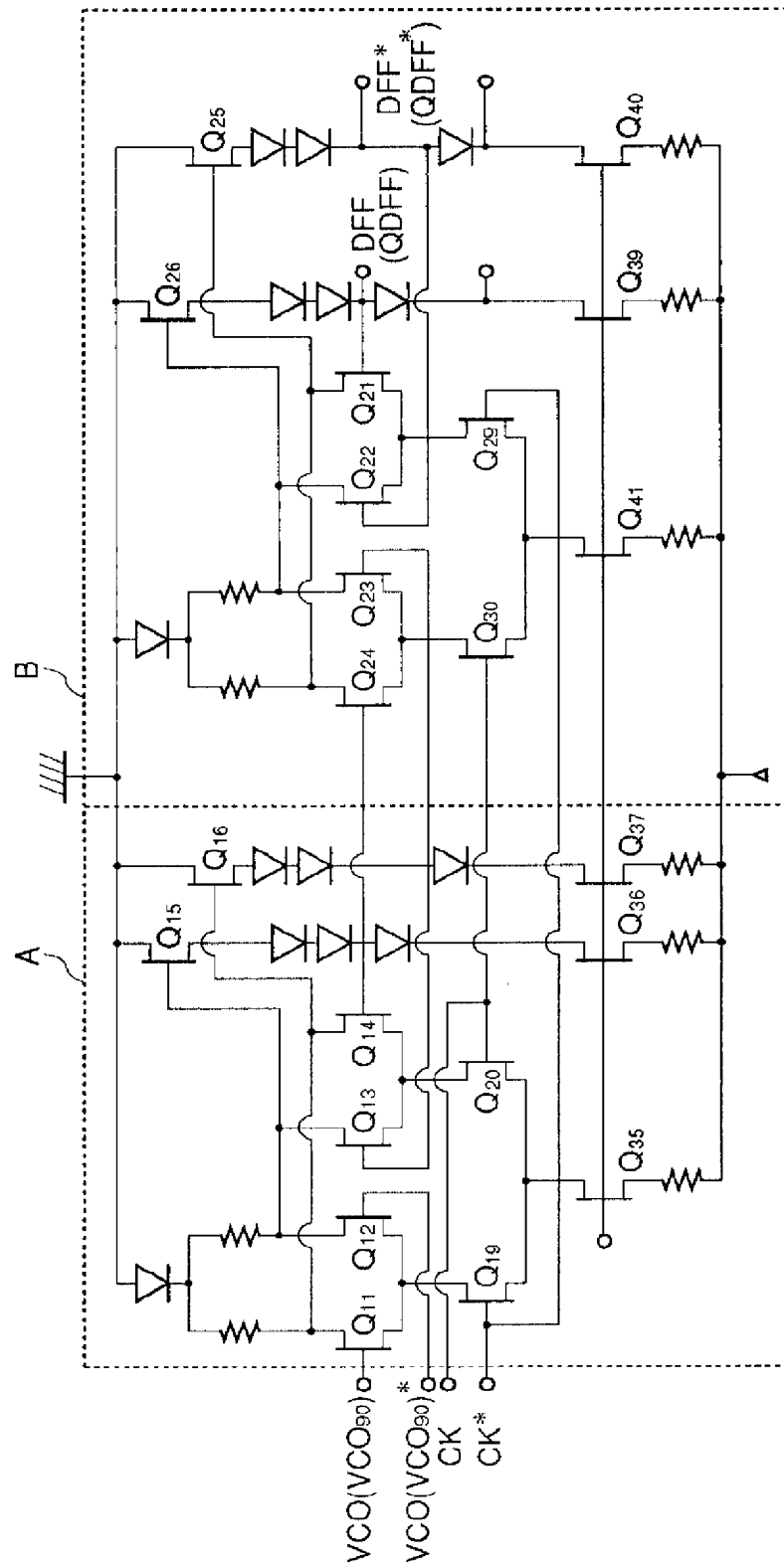
(a)



(b)



【図11】



**\* NOTICES \***

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1. This document has been translated by computer. So the translation may not reflect the original precisely.
2. \*\*\*\* shows the word which can not be translated.
3. In the drawings, any words are not translated.

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**CLAIMS**

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[Claim(s)]

[Claim 1] A phase frequency comparator circuit comprising:

The 1st phase-comparison part that receives a data signal on the basis of a predetermined reference signal and a predetermined clock signal of frequency which a voltage controlled oscillator generates.

A phase converter which shifts a phase of this reference signal 90 degrees.

The 2nd phase-comparison part that receives an output and this data signal of this phase converter.

this -- those sums are outputted in response to one pair of converters of a non-inverter and an opposite phase which change a phase-comparison output of the 1st and 2nd phase-comparison parts into a frequency comparison output, and a phase-comparison output of this phase-comparison part and a frequency comparison output of this converter -- pile up -- a part.

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**DETAILED DESCRIPTION**

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[Detailed Description of the Invention]

[0001]

[Industrial Application] This invention relates to a phase frequency comparator circuit. This invention relates to the composition of the new phase frequency comparator circuit which can be formed as a GaAsMESFET integrated circuit more at details.

[0002]

[Description of the Prior Art] Drawing 9 is a figure showing the typical composition of the conventional phase frequency comparator circuit.

[0003] As shown in the figure, this phase frequency comparator circuit is constituted by three J-K flips-flop 91, 92, and 93.

J terminal input. "OR" They are a  $Q_2$  terminal and a  $Q_3$  terminal by the standup of the taken pulse. "1" It carries out and they are a  $Q_1^*$  terminal and a  $Q_2^*$  terminal at OR of K terminal input. "0" It has composition to carry out.

[0004]

[Problem(s) to be Solved by the Invention] When the above conventional phase frequency comparator circuits are used, in order to constitute a clock data reproduction circuit, for example, the circuit which extracts a clock component from an NRZ-data sequence is needed. It is necessary to input a phase frequency comparison output into a loop filter via a charge pump

circuit. However, it is known that it is difficult to constitute a charge pump circuit from an integrated circuit by GaAsMESFET which has expanded use in recent years.

[0005]Then, this invention solves the problem of the above-mentioned conventional technology, and sets it as the purpose to provide the new phase frequency comparator circuit which can be effectively used also in the integrated circuit by GaAsMESFET.

[0006]

[Means for Solving the Problem]The 1st phase-comparison part that will receive a data signal on the basis of a predetermined reference signal and a predetermined clock signal of frequency which a voltage controlled oscillator generates if this invention is followed, A phase converter which shifts a phase of this reference signal 90 degrees, and the 2nd phase-comparison part that receives an output and this data signal of this phase converter, this -- with one pair of converters of a non-inverter and an opposite phase which change a phase-comparison output of the 1st and 2nd phase-comparison parts into a frequency comparison output. A phase frequency comparator circuit provided with a superposition part which outputs those sums in response to a phase-comparison output of this phase-comparison part and a frequency comparison output of this 1 pair converter is provided.

[0007]

[Function]The phase frequency comparator circuit concerning this invention has the main features in being easy to use and being especially, constituted in a GaAsMESFET integrated circuit, and that there are few high frequency components contained in the output.

[0008]Drawing 1 is a figure showing the fundamental composition of the phase frequency comparator circuit concerning this invention.

[0009]it is shown in the figure -- as -- this circuit -- the 1st phase-comparison part 10 -- pile up -- it mainly comprises the converters 30 and 60 of 20 or 1 pair of part, the 2nd phase-comparison part 40, and the 90-degree phase converter 50. VCO and VCO\* inputted into this circuit in a figure expresses the complementary output of a voltage controlled oscillator, and D and D\* expresses the complementary input data signal. While carrying out phase simulation, frequency  $f_{VCO}$  of VCO and VCO\* and reference clock frequency  $f_D$  of a data signal are in agreement.

[0010]The phase-comparison part 10 receives voltage controlled oscillator output VCO, VCO\* (frequency  $f_{VCO}$ ) and data signal D, and D\* (data rate  $f_D$ ) as it is. The phase-comparison part 40 receives VCO and VCO\* to which the phase shift was shifted 90 degrees by the phase converter 50 with data signal D and D\*. Here, when frequency  $f_{VCO}$  and frequency  $f_D$  are not in agreement, the phase-comparison parts 10 and 40 generate the beat signal of frequency  $|f_{VCO}-f_D|$ . When both are in agreement, the output corresponding to a phase shift occurs.

[0011]Drawing 2 is a figure for explaining the example of composition of a circuit and operation which can be used as the phase-comparison part 10 or 40 in the circuit shown in drawing 1. The numerals as used in the following explanation by which the numerals enclosed in the parenthesis are not surrounded in the signal in the phase-comparison part 40 mean the signal in the phase-comparison part 10, respectively.

[0012]As shown in drawing 2 (a), one pair of latches 11 and 12 and the multiplexer 13 can constitute this phase-comparison part. Voltage controlled oscillator output VCO and VCO\* (VCO<sub>90</sub>, VCO<sub>90</sub>\*) is connected to the latches' 11 and 12 input, and data signal D and D\* is inputted into the latches' 11 and 12 control terminal. Here, data signal D is inputted also into the control terminal of the multiplexer 13. Both each latches' 11 and 12 outputs are connected to the input of the multiplexer 13, and the output of this multiplexer 13 becomes phase-comparison output PD and PD\* (QPD, QPD\*).



[0013]VCO ( $VCO^*$ ) and D ( $D^*$ ) which are inputted into the phase-comparison part constituted as mentioned above have a relation as shown in drawing 2 (b). Therefore, the output of a phase-comparison part changes as follows according to the relation between VCO frequency  $f_{VCO}$  and frequency  $f_D$  of D.

[0014](1) When  $f_{VCO}$  is smaller than  $f_D$  D is a pulse of frequency ( $f_D - f_{VCO}$ ). ;P QPD is the pulse of frequency ( $f_D - f_{VCO}$ ) which the phase followed 90 degrees rather than PD.

(2) When  $f_{VCO}$  is larger than  $f_D$  D is a pulse of frequency ( $f_{VCO} - f_D$ ). ;P QPD is the pulse of frequency ( $f_{VCO} - f_D$ ) which was behind [ PD ] in the phase 90 degrees.

(3) When  $f_{VCO}$  and  $f_D$  are equal and the phase is behind D in the direction of VCO To "H" level, as for D, QPD is "H". It is set to a level. ;P

(4) When  $f_{VCO}$  and  $f_D$  are equal and the phase is behind VCO in the direction of D To an "L" level, as for D, QPD is "H". It is set to a level. ;P

[0015]Drawing 3 is a figure for explaining the basic constitution of a circuit and operation which can be used as the converter 30 or 60 in the circuit shown in drawing 1.

This figure shows the thing equivalent to the converter 30.

[0016]As shown in the figure, one pair of latches 31 and 32 and one pair of NANDs 33 and 34 can constitute a converter. Here, PD and  $PD^*$ , QPD, and  $QPD^*$  is inputted. [ which are the outputs of the phase-comparison parts 10 and 40 at each latches' 31 and 32 input ] PD or  $PD^*$  which is an output of the phase-comparison part 10 is inputted into each latches' 31 and 32 control terminal. The latch's 31 output is inputted into NAND33 with  $PD^*$ . The latch's 32 output is inputted into NAND34 with PD. The output of NANDs 33 and 34 becomes output  $TR_+$  of this converter, and  $TR_+^*$ .

[0017]Although the converter 60 has the same composition fundamentally, it outputs  $TR_-$  and  $TR_-^*$  in response to each signal of PD,  $PD^*$ , QPD, and  $QPD^*$ .

[0018]The output of the converters 30 and 60 constituted as mentioned above changes as follows according to the relation between frequency  $f_{VCO}$  of voltage controlled oscillator output VCO, and frequency  $f_D$  of data signal D.

[0019](1)  $f_{VCO}$  is the pulse which synchronized with  $PD^*$ , respectively, when smaller than  $f_D$ , and;  $TR_+$  are [ PD and  $TR_-$  ]  $TR_+^*$  and  $TR_-^*$ , and "H". It is set to a level.

(2) In  $PD^*$ ,  $f_{VCO}$  of;  $TR_+^*$  is the pulse to which  $TR_-^*$  synchronized with PD, respectively, when larger than  $f_D$ .

$TR_+$  and  $TR_-$ . "H" It is set to a level.

(3) ;(when  $f_{VCO} = f_D$  is approached from state of  $f_{VCO} < f_D$ )  $TR_+$  when  $f_{VCO}$  and  $f_D$  are equal and the phase is behind D in the direction of VCO, Both  $TR_+^*$  and  $TR_-^*$  are. "H" It is set to a level and  $TR_-$  is set to "L" level.

(4) ;(when  $f_{VCO} = f_D$  is approached from state of  $f_{VCO} > f_D$ )  $TR_+$  when  $f_{VCO}$  and  $f_D$  are equal and the phase is behind VCO in the direction of D, Both  $TR_+^*$  and  $TR_-$  are. "H" It is set to a level and  $TR_-^*$  is set to "L" level.

[0020]Drawing 4 is a figure for explaining the composition and operation of a circuit which make repeat mutually in the circuit shown in drawing 1, and can be used as the part 20.

[0021]As shown in the figure, this circuit is constituted combining one pair of unit superposition parts X and Y constituted by the three differential amplifiers 21, 22, and 23 which have one pair of complementary inputs and outputs respectively. That is, in each unit superposition parts X and Y, the inversion input of the differential amplifiers 21 and 23 has received predetermined

reference voltage  $V_{ref}$  in common. The noninverting input of the differential amplifiers 21 and 23 has received output  $TR_+$  of the converter 30,  $TR_+^*$  or output  $TR_-$  of the converter 60, and  $TR_-^*$ . The input of the differential amplifier 22 has received complementary output  $PD^*$  of the phase-comparison part 10, and  $PD$ . On the other hand, after the inverted output of the differential amplifier 22 is added with the inverted output of the differential amplifier 21, it is added with the noninverting output of the differential amplifier 23. After the noninverting output of the differential amplifier 22 is added with the inverted output of the differential amplifier 23, it is added with the noninverting output of the differential amplifier 21. The output of such unit superposition parts X and Y is added still more nearly mutually, and is outputted as the output Q of this superposition part, and  $Q^*$ . Actually, DC-bias-voltage  $V_0$  is further added to each output Q and  $Q^*$ , and is outputted to them.

[0022]It was constituted as mentioned above, and piles up and the output Q of a part and  $Q^*$  change with the relation between frequency  $f_{VCO}$  and frequency  $f_D$ . Drawing 5 is a figure showing the output Q of this circuit and  $Q^*$  which change with the relation between frequency  $f_{VCO}$  and frequency  $f_D$ .

[0023]The output level of each amplifiers 21, 22, and 23 in each state is shown in Table 1.

[0024]

[Table 1]

| 出力レベル    | "H" レベル   | "L" レベル    |
|----------|-----------|------------|
| 増幅器21、23 | $V_{of}$  | $-V_{of}$  |
| 増幅器22    | $2V_{of}$ | $-2V_{of}$ |

[0025]When smaller than  $f_D$  (shown in drawing 5 (a)),  $f_{VCO}$  (1) ;  $Q=V_0-V_{of}$ ,  $Q^*=V_0+V_{of}$  (2)  $f_{VCO}$ ;  $Q=V_0+V_{of}$  when larger than  $f_D$  (shown in drawing 5 (a)), When  $Q^*=V_0-[V_{of}]$  (3)  $f_{VCO}$  and  $f_D$  are equal and the phase is behind D in the direction of  $VCO$ ; (when  $f_{VCO}=f_D$  is approached from the state of  $f_{VCO}<f_D$ )  $Q=V_0-V_{of}$  shown in drawing 5 (c), and  $Q=V_0+V_{of}$  (4)  $f_{VCO}$  and  $f_D$  are equal, ;(when  $f_{VCO}=f_D$  is approached from state of  $f_{VCO}>f_D$ , shown in drawing 5 (d))  $Q=V_0+V_{of}$ , and  $Q=V_0-V_{of}$  when the phase is behind VCO in the direction of D [0026]The phase frequency comparator circuit concerning this invention constituted as mentioned above can generate the control signal for performing phase simulation control whose phase and frequency of a voltage controlled oscillator correspond by adding a loop filter immediately after that.

[0027]An expected function can be realized in this method, without adding the circuit for extracting a clock component from a data signal, a charge pump circuit, etc. Therefore, constituting a charge pump circuit can use it also in a difficult GaAsMESFET integrated circuit.

[0028]In the composition of this phase frequency comparator, no high frequency component which originates in a beat signal etc. in the frequency level-luffing-motion process from an asynchronous time is outputted so that drawing 5 may also show. Therefore, there is no possibility that malfunction of the phase shift synchronous loop resulting from the high frequency component of an output signal may arise. As shown in

drawing 5(c), this phase frequency comparator circuit has an ideal output wave, and the design of the phase-locked loop linked to this is easy.

[0029]If one mode of this invention is followed, in the phase frequency comparator circuit shown in drawing 1, a D type flip-flop can also constitute the phase-comparison parts 10 and 40. Drawing 10 is a figure for explaining the function of the phase-comparison part constituted using a D type flip-flop.

[0030]As shown in drawing 10 (a), to a D type flip-flop, output VCO of a voltage controlled oscillator and VCO are inputted into data input, and the reference clock signal of data is inputted into the control input of a D type flip-flop. Here, VCO (VCO) and clock signal CK (CK) which are inputted into a D type flip-flop have a relation as shown in drawing 10 (b). Therefore, the output DFF of a phase-comparison part changes with frequency fVCO of VCO, and frequency fCK of clock signal CK as follows.

[0031](1) In;DFF, fVCO is a pulse of frequency (fCK-fVCO), when smaller than fCK. QDFF is the pulse of frequency (fCK-fVCO) which the phase followed 90 degrees rather than DFF.

(2) In;DFF, fVCO is a pulse of frequency (fVCO-fCK), when larger than fCK. QDFF is the pulse of frequency (fVCO-fCK) which was behind [ DFF ] in the phase 90 degrees.

(3) When fVCO and fCK are equal and the phase is behind D in the direction of VCO; as for DFF, QDFF is "L" to "H" level. It is set to a level.

(4) When fVCO and fCK are equal and the phase is behind VCO in the direction of D; as for DFF, QDFF is "L" to "L" level. It is set to a level.

[0032]Therefore, a D type flip-flop is used as the phase-comparison parts 10 and 40 of the phase frequency comparator circuit shown in drawing 1. Instead of output PD [ of the phase-comparison parts 10 and 40 ], PD, QPD, and QPD, this phase frequency comparison part operates like the case where the composition shown in drawing 1 is already explained, by using output [ of a D type flip-flop ] DFF, DFF, QDFF, and QDFF.

However, in this composition, clock signal CK for supplying a D type flip-flop is needed.

[0033]Hereafter, although this invention is concretely explained with reference to an example, the following indications are only one example of this invention, and do not limit the technical scope of this invention at all.

[0034]

[Example]Drawing 6 is a figure showing the more concrete example of composition of the phase-comparison part shown in drawing 2.

[0035]1 pair each of FETQ11-Q12 and Q21-Q22 from which each input edge of this circuit receives output VCO with a complementary voltage controlled oscillator, and VCO in a gate, respectively as shown in the figure, It has 1 pair of FETQ31-Q32 which receives data signal D and D in a gate.

[0036]To FET pair Q11-Q12 and Q21-Q22. FETQ15, FETQ14 to which the current path containing Q25 was connected at the gate, FETQ13 by which the current path to which Q24 contains FETQ16 and Q26 in a FETQ11 and Q21 side was connected to the gate, and Q23 are connected to the FETQ12 and Q22 side, respectively.

[0037]The gate of FETQ18 and Q28 is connected to the current path in which the gate of FETQ17 and Q27 contains FETQ16 and Q26 in the current path containing FETQ15 and Q25, respectively. The end of FETQ17 and Q27 to the gate of FETQ33. The end of FETQ18 and Q18 is connected to the gate of FETQ34, respectively, and the outgoing end of this circuit is constituted by FETQ33, Q34, and the level shift diode group. The gate of FETQ19 and the gate of Q29 are connected mutually.

[0038]Only data signal D is impressed also to the gate of FETQ20 and Q30 as a control signal of a multiplexer. FET pair Q19-Q20 and Q31-Q32 and Q29-Q30 and FETQ15, Q16, Q25, Q26, Q33, and Q34 are individually provided with the current source constituted by FETQ35 - Q43, respectively.

[0039]In the circuit constituted as mentioned above, if either of the FETQ11-Q21 and Q12-Q22 flows by voltage controlled oscillator output VCO and VCO<sub>\*</sub>, according to it, either of the FETQ16-Q26 and Q15-Q25 will flow. If either of the FETQ16-Q26 and Q15-Q25 flows, Q14-Q17-Q24-Q27 either one of FETQ13-Q18-Q23-Q28 or will flow. Here Each FET pair Q13-Q14 and Q17-Q18, Since it becomes effective alternatively according to data signal D and D<sub>\*</sub>, Q21-Q22 and FET pair Q11-Q12 and Q23-Q24 and Q27-Q28 flow through FETQ33 and Q34 alternatively. That is, voltage controlled oscillator output VCO and VCO<sub>\*</sub> is latched by data signal D and D<sub>\*</sub>, and is further outputted according to data signal D and D<sub>\*</sub>. Therefore, a complementary phase-comparison output is obtained by output PD and PD<sub>\*</sub>.

[0040]Drawing 11 is a figure showing the concrete example of composition of the phase-comparison part at the time of using the D type flip-flop shown in drawing 10.

[0041]As shown in the figure, this circuit serves as 2 stage constitution of the circuit A of the same composition, and the circuit B mutually.

The input of the circuit A receives voltage controlled oscillator output VCO and VCO<sub>\*</sub>, and the input of the circuit B has undergone the output of the circuit A, respectively.

The input edge of circuit A (B) is constituted by 1 pair of FETQ11-Q12 (Q21-Q22) which receives an input signal in a gate, and 1 pair each of FETQ19-Q20 (Q29-Q30) which receives clock signal CK and CK<sub>\*</sub> in a gate. FET pair Q19-Q20 (Q29-Q30) and FETQ15, and Q16 (Q25, Q26) are provided with the current source constituted by FETQ35 - Q37 (Q39-Q41), respectively.

[0042]The gate of FETQ13 (Q23) is connected to the current path in which the gate of FETQ14 (Q24) contains FETQ16 (Q26) in the current path containing FETQ15 (Q25), respectively. The end of FETQ14 (Q24) is connected to the end of FETQ11 (Q21), and the FETQ13 (Q13) end is connected to the end of FETQ12 (Q22), respectively. Therefore, since FETQ16 (Q26) will flow and it will flow also through FETQ13 (Q13) at this time if FETQ11 (Q21) flows, for example, a complementary output occurs in the outgoing end of circuit A (B). The outgoing end of this circuit A (B) is connected to the end of FETQ15 (Q25) and Q16 (Q26) via the diode group.

[0043]The circuit constituted as mentioned above is a typical D type flip-flop.

The function is as having already explained with reference to drawing 10.

Therefore, it can be used in the circuit concerning this invention, being able to replace with the phase-comparison part shown in drawing 6.

[0044]Drawing 7 is a figure showing the example of the converter 30 in the circuit shown in drawing 1.

[0045]As shown also in drawing 3, this circuit comprises a NAND gate which takes NAND of one pair of latch circuitry which latches the output QPD of the phase-comparison part 40, and QPD, and each latch's output and PD and PD by output PD of the phase-comparison part 10, and PD. Therefore, except for having received output PD of the phase-comparison part 10, and PD instead of data signal D and D as compared with drawing 6, and having received the output QPD of the phase-comparison part 40, and QPD instead of voltage controlled oscillator output VCO and VCO, the composition of latch circuitry is common. On the other hand, in the portion relevant to two pairs of FETQ51-Q52 and Q53-Q54 and outgoing ends equivalent to the NAND circuit of drawing 3, this circuit has original composition.

[0046]That is, each FET pair Q51-Q52 and Q53-Q54 receives the output of each latch circuitry in a gate, and it is constituted so that output PD of the phase-comparison part 10 and PD may validate selectively. Therefore, from the output of FET pair Q51-Q52 and Q53-Q54, the complementary transform signal TR and TR are outputted mutually.

[0047]Drawing 8 is a figure in which making it put each other and showing the concrete example of composition of a part.

[0048]The three differential amplifiers 21, 22, and 23 with which this circuit was respectively constituted by one pair of FETQ61 - Q66 as shown in the figure, It comprises the current source part 81 constituted by FETQ67 - Q69, respectively combining one pair of unit superposition parts X and Y which each comprised.

[0049]One output of the differential amplifier 22 is combined with the output of one way each of the differential amplifiers 21 and 23 in each unit superposition parts X and Y.

The output of another side of each differential amplifiers 21, 22, and 23 is also combined mutually.

Each differential amplifiers 21, 22, and 23 are connected to the current source 81 by FETQ67 - Q69, respectively. each -- it is such -- composition -- having -- a unit -- superposition -- a part -- X -- Y -- mutual -- an output -- joining together -- having -- while -- further -- resistance -- R -- ' -- R -- -- zero -- -- ' -- a diode group -- D -- -- zero -- -- ' -- and -- FETQ -- -- zero -- -- ' -- constituting -- having had -- a reference voltage generating part -- G -- common -- connecting -- having -- \*\*\*\*.

[0050]It was constituted as mentioned above, and piles up and output signal PD of the phase-comparison part 10 and PD are impressed to each gate of FETQ64 and Q63 which is one pair of inputs of the differential amplifier 22 in the unit superposition part X in a part. Output TR+ of the converter 30 and TR+ are impressed to the gate of FETQ61 of the differential amplifier 21, and the gate of FETQ66 of the differential amplifier 23, respectively. The reference voltage which the reference voltage generating part G generates is impressed to the gate of FETQ62 of the differential amplifier 21, and FETQ65 of the differential amplifier 23.

[0051]On the other hand, in the unit superposition part Y, output signal PD of the phase-comparison part 10

\*  
and PD<sup>\*</sup> are impressed to each gate of FETQ64 and Q63<sup>\*</sup> which is one pair of inputs of the differential amplifier 22. Output TR<sup>-</sup> of the converter 60 and TR<sup>-</sup> are impressed to the gate of FETQ61 of the differential amplifier 21, and the gate of FETQ66 of the differential amplifier 23, respectively. The reference voltage which the reference voltage generating part G generates is impressed to the gate of FETQ62 of the differential amplifier 21, and FETQ65 of the differential amplifier 23.

[0052]In the circuit constituted as mentioned above, that to which the sum of signal PD, PD<sup>\*</sup> and signal TR<sup>+</sup>, and TR<sup>+</sup> and the sum of signal PD, PD<sup>\*</sup> and signal TR<sup>-</sup>, and TR<sup>-</sup> were added further is outputted as the signal Q and Q<sup>\*</sup>.

[0053]In the reference voltage generating part G of the circuit shown in drawing 7 and drawing 8, as shown in a figure, When gate width of D0 and FET is made into Q0 for R0, R1, and the anode width of a diode, the resistance of resistance, Stable reference voltage can be generated to a temperature change and line voltage variation with easy composition Q0' and by producing so that D0' and R0' may satisfy the following formula 1 and the formula 2, respectively.

[0054]

[Formula 1]

$Q0' = nQ0$ ,  $D0' = nD0$ ,  $R1' = (1/n) R1$  [0055]

[Formula 2]  $R0' - I0' = R0 - I0 + R0I1/2$  [0056]

[Effect of the Invention]As explained above, the phase frequency comparator circuit by this invention does not need to provide separately the circuit which extracts a clock component from a data signal to the phase-locked loop for clock data circuits. A charge pump circuit is not needed between loop filters. Therefore, in the GaAsMESFET integrated circuit which cannot constitute especially a charge pump easily, it can be used advantageously.

[0057]In the phase frequency comparator concerning this invention, since no high frequency component which originates in a beat signal etc. in the frequency level-luffing-motion process from an asynchronous time is outputted, there is no possibility that malfunction of the phase shift synchronous loop resulting from the high frequency component of an output signal may arise. For this reason, it is effective in the design of the phase-locked loop linked to this phase frequency comparator circuit becoming easy.

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## TECHNICAL FIELD

[Industrial Application]This invention relates to a phase frequency comparator circuit. This invention relates to the composition of the new phase frequency comparator circuit which can be formed as a GaAsMESFET integrated circuit more at details.

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## PRIOR ART

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[Description of the Prior Art]Drawing 9 is a figure showing the typical composition of the conventional phase frequency comparator circuit.

[0003]As shown in the figure, this phase frequency comparator circuit is constituted by three J-K flips-flop 91, 92, and 93.

J terminal input. "OR" They are a  $Q_2$  terminal and a  $Q_3$  terminal by the standup of the taken pulse. "1" It carries out and they are a  $Q_1^*$  terminal and a  $Q_2^*$  terminal at OR of K terminal input. "0" It has composition to carry out.

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## EFFECT OF THE INVENTION

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[Effect of the Invention]As explained above, the phase frequency comparator circuit by this invention does not need to provide separately the circuit which extracts a clock component from a data signal to the phase-locked loop for clock data circuits. A charge pump circuit is not needed between loop filters. Therefore, in the GaAsMESFET integrated circuit which cannot constitute especially a charge pump easily, it can be used advantageously.

[0057]In the phase frequency comparator concerning this invention, since no high frequency component which originates in a beat signal etc. in the frequency level-luffing-motion process from an asynchronous time is outputted, there is no possibility that malfunction of the phase shift synchronous loop resulting from the high frequency component of an output signal may arise. For this reason, it is effective in the design of the phase-locked loop linked to this phase frequency comparator circuit becoming easy.

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## TECHNICAL PROBLEM

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[Problem(s) to be Solved by the Invention]When the above conventional phase frequency comparator circuits are used, in order to constitute a clock data reproduction circuit, for example, the circuit which extracts a clock component from an NRZ-data sequence is needed. It is necessary to input a phase frequency comparison output into a loop filter via a charge pump circuit. However, it is known that it is difficult to constitute a charge pump circuit from an integrated circuit by GaAsMESFET which has expanded use in recent years.

[0005]Then, this invention solves the problem of the above-mentioned conventional technology, and sets it as the purpose to provide the new phase frequency comparator circuit which can be effectively used also in the integrated circuit by GaAsMESFET.

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## MEANS

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[Means for Solving the Problem]The 1st phase-comparison part that will receive a data signal on the basis of a predetermined reference signal and a predetermined clock signal of frequency which a voltage controlled oscillator generates if this invention is followed, A phase converter which shifts a phase of this reference signal 90 degrees, and the 2nd phase-comparison part that receives an output and this data signal of this phase converter, this -- with one pair of converters of a non-inverter and an opposite phase which change a phase-comparison output of the 1st and 2nd phase-comparison parts into a frequency comparison output. A phase frequency comparator circuit provided with a superposition part which outputs those sums in response to a phase-comparison output of this phase-comparison part and a frequency comparison output of this 1 pair converter is provided.

## OPERATION

[Function]The phase frequency comparator circuit concerning this invention has the main features in being easy to use and being especially, constituted in a GaAsMESFET integrated circuit, and that there are few high frequency components contained in the output.

[0008]Drawing 1 is a figure showing the fundamental composition of the phase frequency comparator circuit concerning this invention.

[0009]it is shown in the figure -- as -- this circuit -- the 1st phase-comparison part 10 -- pile up -- it mainly comprises the converters 30 and 60 of 20 or 1 pair of part, the 2nd phase-comparison part 40, and the 90-degree phase converter 50. VCO and VCO\* inputted into this circuit in a figure expresses the complementary output of a voltage controlled oscillator, and D and D\* expresses the complementary input data signal. While carrying out phase simulation, frequency  $f_{VCO}$  [of VCO and VCO\*] and reference clock frequency  $f_D$  of a data signal are in agreement.

[0010]The phase-comparison part 10 receives voltage controlled oscillator output VCO, VCO\* (frequency  $f_{VCO}$ ) and data signal D, and D\* (data rate  $f_D$ ) as it is. The phase-comparison part 40 receives VCO and VCO\* to which the phase shift was shifted 90 degrees by the phase converter 50 with data signal D and D\*. Here, when frequency  $f_{VCO}$  and frequency  $f_D$  are not in agreement, the phase-comparison parts 10 and 40 generate the beat signal of frequency  $|f_{VCO}-f_D|$ . When both are in agreement, the output corresponding to a phase shift occurs.

[0011]Drawing 2 is a figure for explaining the example of composition of a circuit and operation which can be used as the phase-comparison part 10 or 40 in the circuit shown in drawing 1. The numerals as used in the following explanation by which the numerals enclosed in the parenthesis are not surrounded in the signal in the phase-comparison part 40 mean the signal in the phase-comparison part 10, respectively.

[0012]As shown in drawing 2 (a), one pair of latches 11 and 12 and the multiplexer 13 can constitute this phase-comparison part. Voltage controlled oscillator output VCO and VCO\* (VCO<sub>90</sub>, VCO<sub>90</sub>\*) is connected to the latches' 11 and 12 input, and data signal D and D\* is inputted into the latches' 11 and 12 control terminal. Here, data signal D is inputted also into the control terminal of the multiplexer 13. Both each latches' 11 and 12 outputs are connected to the input of the multiplexer 13, and the output of this multiplexer 13 becomes phase-comparison output PD and PD\* (QPD, QPD\*).

[0013]VCO (VCO\*) and D (D\*) which are inputted into the phase-comparison part constituted as mentioned above have a relation as shown in drawing 2 (b). Therefore, the output of a phase-comparison part changes as follows according to the relation between VCO frequency  $f_{VCO}$  and frequency  $f_D$  of D.

[0014](1) When  $f_{VCO}$  is smaller than  $f_D$  D is a pulse of frequency  $(f_D-f_{VCO})$ . ;P QPD is the pulse of frequency  $(f_D-f_{VCO})$  which the phase followed 90 degrees rather than PD.

(2) When  $f_{VCO}$  is larger than  $f_D$  D is a pulse of frequency  $(f_{VCO}-f_D)$ . ;P QPD is the pulse of frequency  $(f_{VCO}-f_D)$  which was behind [ PD ] in the phase 90 degrees.

(3) When  $f_{VCO}$  and  $f_D$  are equal and the phase is behind D in the direction of VCO To "H" level, as for D, QPD is "H". It is set to a level. ;P

(4) When  $f_{VCO}$  and  $f_D$  are equal and the phase is behind VCO in the direction of D To an "L" level, as for D, QPD is "H". It is set to a level. ;P

[0015]Drawing 3 is a figure for explaining the basic constitution of a circuit and operation which can be used as the converter 30 or 60 in the circuit shown in drawing 1.



This figure shows the thing equivalent to the converter 30.

[0016]As shown in the figure, one pair of latches 31 and 32 and one pair of NANDs 33 and 34 can constitute a converter. Here, PD and PD\*, QPD, and QPD\* is inputted. [ which are the outputs of the phase-comparison parts 10 and 40 at each latches' 31 and 32 input ] PD or PD\* which is an output of the phase-comparison part 10 is inputted into each latches' 31 and 32 control terminal. The latch's 31 output is inputted into NAND33 with PD\*. The latch's 32 output is inputted into NAND34 with PD. The output of NANDs 33 and 34 becomes output TR<sub>+</sub> of this converter, and TR<sub>+</sub>\*.

[0017]Although the converter 60 has the same composition fundamentally, it outputs TR<sub>-</sub> and TR<sub>-</sub>\* in response to each signal of PD, PD\*, QPD, and QPD\*.

[0018]The output of the converters 30 and 60 constituted as mentioned above changes as follows according to the relation between frequency f<sub>VCO</sub> of voltage controlled oscillator output VCO, and frequency f<sub>D</sub> of data signal D.

[0019](1) f<sub>VCO</sub> is the pulse which synchronized with PD\*, respectively, when smaller than f<sub>D</sub>, and; TR<sub>+</sub> are [ PD and TR<sub>-</sub> ] TR<sub>+</sub>\* and TR<sub>-</sub>\*, and "H". It is set to a level.

(2) In PD\*, f<sub>VCO</sub> of; TR<sub>+</sub>\* is the pulse to which TR<sub>-</sub>\* synchronized with PD, respectively, when larger than f<sub>D</sub>.

TR<sub>+</sub> and TR<sub>-</sub>. "H" It is set to a level.

(3) ;(when f<sub>VCO</sub>=f<sub>D</sub> is approached from state of f<sub>VCO</sub><f<sub>D</sub>) TR<sub>+</sub> when f<sub>VCO</sub> and f<sub>D</sub> are equal and the phase is behind D in the direction of VCO, Both TR<sub>+</sub>\* and TR<sub>-</sub>\* are. "H" It is set to a level and TR<sub>-</sub> is set to "L" level.

(4) ;(when f<sub>VCO</sub>=f<sub>D</sub> is approached from state of f<sub>VCO</sub>>f<sub>D</sub>) TR<sub>+</sub> when f<sub>VCO</sub> and f<sub>D</sub> are equal and the phase is behind VCO in the direction of D, Both TR<sub>+</sub>\* and TR<sub>-</sub> are. "H" It is set to a level and TR<sub>-</sub>\* is set to "L" level.

[0020]Drawing 4 is a figure for explaining the composition and operation of a circuit which make repeat mutually in the circuit shown in drawing 1, and can be used as the part 20.

[0021]As shown in the figure, this circuit is constituted combining one pair of unit superposition parts X and Y constituted by the three differential amplifiers 21, 22, and 23 which have one pair of complementary inputs and outputs respectively. That is, in each unit superposition parts X and Y, the inversion input of the differential amplifiers 21 and 23 has received predetermined reference voltage V<sub>ref</sub> in common. The noninverting input of the differential amplifiers 21 and 23 has received output TR<sub>+</sub> of the converter 30, TR<sub>+</sub>\* or output TR<sub>-</sub> of the converter 60, and TR<sub>-</sub>\*. The input of the differential amplifier 22 has received complementary output PD\* of the phase-comparison part 10, and PD. On the other hand, after the inverted output of the differential amplifier 22 is added with the inverted output of the differential amplifier 21, it is added with the noninverting output of the differential amplifier 23. After the noninverting output of the differential amplifier 22 is added with the inverted output of the differential amplifier 23, it is added with the noninverting output of the differential amplifier 21. The output of such unit superposition parts X and Y is added still more nearly mutually, and is outputted as the output Q of this superposition part, and Q\*. Actually, DC-bias-voltage V<sub>0</sub> is further added to each output Q and Q\*, and is outputted to them.

[0022]It was constituted as mentioned above, and piles up and the output Q of a part and Q\* change with the relation between frequency f<sub>VCO</sub> and frequency f<sub>D</sub>. Drawing 5 is a figure showing the output Q of this circuit and Q\* which change with the relation between frequency

$f_{VCO}$  and frequency  $f_D$ .

[0023]The output level of each amplifiers 21, 22, and 23 in each state is shown in Table 1.

[0024]

[Table 1]

| 出力レベル    | "H" レベル   | "L" レベル    |
|----------|-----------|------------|
| 増幅器21、23 | $V_{of}$  | $-V_{of}$  |
| 増幅器22    | $2V_{of}$ | $-2V_{of}$ |

[0025]When smaller than  $f_D$  (shown in drawing 5 (a)),  $f_{VCO}$  (1);  $Q=V_0-V_{of}$ ,  $Q^*=V_0+V_{of}$  (2)

$f_{VCO}$ ;  $Q=V_0+V_{of}$  when larger than  $f_D$  (shown in drawing 5 (a)), When  $Q^*=V_0-[V_{of}]$  (3)  $f_{VCO}$  and  $f_D$  are

equal and the phase is behind D in the direction of VCO; (when  $f_{VCO}=f_D$  is approached from the state of  $f_{VCO}<f_D$ )  $Q=V_0-V_{of}$  shown in

drawing 5 (c), and  $Q^*=V_0+V_{of}$  (4)  $f_{VCO}$  and  $f_D$  are equal, (when  $f_{VCO}=f_D$  is approached from state of  $f_{VCO}>f_D$ , shown in drawing 5 (d))

$Q=V_0+V_{of}$ , and  $Q^*=V_0-V_{of}$  when the phase is behind VCO in the direction of D [0026]The phase frequency comparator circuit concerning this invention constituted as mentioned above can generate the control signal for performing phase simulation control whose phase and frequency of a voltage controlled oscillator correspond by adding a loop filter immediately after that.

[0027]An expected function can be realized in this method, without adding the circuit for extracting a clock component from a data signal, a charge pump circuit, etc. Therefore, constituting a charge pump circuit can use it also in a difficult GaAsMESFET integrated circuit.

[0028]In the composition of this phase frequency comparator, no high frequency component which originates in a beat signal etc. in the frequency level-luffing-motion process from an asynchronous time is outputted so that drawing 5 may also show. Therefore, there is no possibility that malfunction of the phase shift synchronous loop resulting from the high frequency component of an output signal may arise. As shown in drawing 5 (c), this phase frequency comparator circuit has an ideal output wave, and the design of the phase-locked loop linked to this is easy.

[0029]If one mode of this invention is followed, in the phase frequency comparator circuit shown in drawing 1, a D type flip-flop can also constitute the phase-comparison parts 10 and 40. Drawing 10 is a figure for explaining the function of the phase-comparison part constituted using a D type flip-flop.

[0030]As shown in drawing 10 (a), to a D type flip-flop, output VCO of a voltage controlled oscillator and  $VCO^*$  are inputted into data input, and the reference clock signal of data is inputted into the control input of a D type flip-flop. Here, VCO ( $VCO^*$ ) and clock signal CK ( $CK^*$ ) which are inputted into a D type flip-flop have a relation as shown in drawing 10 (b). Therefore, the output DFF of a phase-comparison part changes with frequency  $f_{VCO}$  of VCO, and frequency  $f_{CK}$  of clock signal CK as follows.

[0031](1) In; DFF,  $f_{VCO}$  is a pulse of frequency ( $f_{CK}-f_{VCO}$ ), when smaller than  $f_{CK}$ . QDFF is the pulse of frequency ( $f_{CK}-f_{VCO}$ ) which the phase followed 90 degrees rather than DFF.

(2) In; DFF,  $f_{VCO}$  is a pulse of frequency ( $f_{VCO}-f_{CK}$ ), when larger than  $f_{CK}$ . QDFF is the pulse of frequency ( $f_{VCO}-f_{CK}$ ) which was behind [DFF] in the phase 90 degrees.

(3) When  $f_{VCO}$  and  $f_{CK}$  are equal and the phase is behind D in the direction of VCO; as for DFF, QDFF is "L" to "H" level. It is set to a level.

(4) When  $f_{VCO}$  and  $f_{CK}$  are equal and the phase is behind VCO in the direction of D; as for DFF, QDFF is "L" to "L" level. It is set to a level.

[0032]Therefore, a D type flip-flop is used as the phase-comparison parts 10 and 40 of the phase frequency comparator circuit shown in drawing 1. Instead of output PD [of the phase-comparison parts 10 and 40], PD, QPD, and QPD, this phase frequency comparison part operates like the case where the composition shown in drawing 1 is already explained, by using output [of a D type flip-flop] DFF, DFF, QDFF, and QDFF. However, in this composition, clock signal CK for supplying a D type flip-flop is needed.

[0033]Hereafter, although this invention is concretely explained with reference to an example, the following indications are only one example of this invention, and do not limit the technical scope of this invention at all.

## EXAMPLE

[Example] Drawing 6 is a figure showing the more concrete example of composition of the phase-comparison part shown in drawing 2.

[0035] 1 pair each of FETQ<sub>11</sub>-Q<sub>12</sub> and Q<sub>21</sub>-Q<sub>22</sub> from which each input edge of this circuit receives output VCO with a complementary voltage controlled oscillator, and VCO\* in a gate, respectively as shown in the figure, It has 1 pair of FETQ<sub>31</sub>-Q<sub>32</sub> which receives data signal D and D\* in a gate.

[0036] To FET pair Q<sub>11</sub>-Q<sub>12</sub> and Q<sub>21</sub>-Q<sub>22</sub>. FETQ<sub>15</sub>, FETQ<sub>14</sub> to which the current path containing Q<sub>25</sub> was connected at the gate, FETQ<sub>13</sub> by which the current path to which Q<sub>24</sub> contains FETQ<sub>16</sub> and Q<sub>26</sub> in a FETQ<sub>11</sub> and Q<sub>21</sub> side was connected to the gate, and Q<sub>23</sub> are connected to the FETQ<sub>12</sub> and Q<sub>22</sub> side, respectively.

[0037] The gate of FETQ<sub>18</sub> and Q<sub>28</sub> is connected to the current path in which the gate of FETQ<sub>17</sub> and Q<sub>27</sub> contains FETQ<sub>16</sub> and Q<sub>26</sub> in the current path containing FETQ<sub>15</sub> and Q<sub>25</sub>, respectively. The end of FETQ<sub>17</sub> and Q<sub>27</sub> to the gate of FETQ<sub>33</sub>. The end of FETQ<sub>18</sub> and Q<sub>18</sub> is connected to the gate of FETQ<sub>34</sub>, respectively, and the outgoing end of this circuit is constituted by FETQ<sub>33</sub>, Q<sub>34</sub>, and the level shift diode group. The gate of FETQ<sub>19</sub> and the gate of Q<sub>29</sub> are connected mutually.

[0038] Only data signal D is impressed also to the gate of FETQ<sub>20</sub> and Q<sub>30</sub> as a control signal of a multiplexer. FET pair Q<sub>19</sub>-Q<sub>20</sub> and Q<sub>31</sub>-Q<sub>32</sub> and Q<sub>29</sub>-Q<sub>30</sub> and FETQ<sub>15</sub>, Q<sub>16</sub>, Q<sub>25</sub>, Q<sub>26</sub>, Q<sub>33</sub>, and Q<sub>34</sub> are individually provided with the current source constituted by FETQ<sub>35</sub> - Q<sub>43</sub>, respectively.

[0039] In the circuit constituted as mentioned above, if either of the FETQ<sub>11</sub>-Q<sub>21</sub> and Q<sub>12</sub>-Q<sub>22</sub> flows by voltage controlled oscillator output VCO and VCO\*, according to it, either of the FETQ<sub>16</sub>-Q<sub>26</sub> and Q<sub>15</sub>-Q<sub>25</sub> will flow. If either of the FETQ<sub>16</sub>-Q<sub>26</sub> and Q<sub>15</sub>-Q<sub>25</sub> flows, Q<sub>14</sub>-Q<sub>17</sub>-Q<sub>24</sub>-Q<sub>27</sub> either one of FETQ<sub>13</sub>-Q<sub>18</sub>-Q<sub>23</sub>-Q<sub>28</sub> or will flow. Here Each FET pair Q<sub>13</sub>-Q<sub>14</sub> and Q<sub>17</sub>-Q<sub>18</sub>, Since it becomes effective alternatively according to data signal D and D\*, Q<sub>21</sub>-Q<sub>22</sub> and FET pair Q<sub>11</sub>-Q<sub>12</sub> and Q<sub>23</sub>-Q<sub>24</sub> and Q<sub>27</sub>-Q<sub>28</sub> flow through FETQ<sub>33</sub> and Q<sub>34</sub> alternatively. That is, voltage controlled oscillator output VCO and VCO\* is latched by data signal D and D\*, and is further outputted according to data signal D and D\*. Therefore, a complementary phase-comparison output is obtained by output PD and PD\*.

[0040] Drawing 11 is a figure showing the concrete example of composition of the phase-comparison part at the time of using the D type flip-flop shown in drawing 10.

[0041] As shown in the figure, this circuit serves as 2 stage constitution of the circuit A of the same composition, and the circuit B mutually.

The input of the circuit A receives voltage controlled oscillator output VCO and VCO\*, and the input of the circuit B has undergone the output of the circuit A, respectively.

The input edge of circuit A (B) is constituted by 1 pair of FETQ<sub>11</sub>-Q<sub>12</sub> (Q<sub>21</sub>-Q<sub>22</sub>) which receives an input signal in a gate, and 1 pair each of FETQ<sub>19</sub>-Q<sub>20</sub> (Q<sub>29</sub>-Q<sub>30</sub>) which receives clock signal CK and CK\* in a gate. FET pair Q<sub>19</sub>-Q<sub>20</sub> (Q<sub>29</sub>-Q<sub>30</sub>) and FETQ<sub>15</sub>, and Q<sub>16</sub> (Q<sub>25</sub>, Q<sub>26</sub>) are provided with the current source constituted by FETQ<sub>35</sub> - Q<sub>37</sub> (Q<sub>39</sub>-Q<sub>41</sub>), respectively.

[0042] The gate of FETQ<sub>13</sub> (Q<sub>23</sub>) is connected to the current path in which the gate of FETQ<sub>14</sub> (Q<sub>24</sub>) contains FETQ<sub>16</sub> (Q<sub>26</sub>) in the current path containing FETQ<sub>15</sub> (Q<sub>25</sub>), respectively. The end of FETQ<sub>14</sub> (Q<sub>24</sub>) is connected to the end of FETQ<sub>11</sub> (Q<sub>21</sub>), and the FETQ<sub>13</sub> (Q<sub>13</sub>) end is connected to the end of FETQ<sub>12</sub> (Q<sub>22</sub>), respectively. Therefore, since FETQ<sub>16</sub> (Q<sub>26</sub>) will flow and it will flow also through FETQ<sub>13</sub> (Q<sub>13</sub>) at this time if FETQ<sub>11</sub> (Q<sub>21</sub>) flows, for example, a complementary output occurs in the outgoing end of circuit A (B). The outgoing end of this circuit A (B) is connected to the end of FETQ<sub>15</sub> (Q<sub>25</sub>) and Q<sub>16</sub> (Q<sub>26</sub>) via the diode group.

[0043]The circuit constituted as mentioned above is a typical D type flip-flop.

The function is as having already explained with reference to drawing 10.

Therefore, it can be used in the circuit concerning this invention, being able to replace with the phase-comparison part shown in drawing 6.

[0044]Drawing 7 is a figure showing the example of the converter 30 in the circuit shown in drawing 1.

[0045]As shown also in drawing 3, this circuit comprises a NAND gate which takes NAND of one pair of latch circuitry which latches the output QPD of the phase-comparison part 40, and QPD\*, and each latch's output and PD and PD\* by output PD of the phase-comparison part 10, and PD\*. Therefore, except for having received output PD of the phase-comparison part 10, and PD\* instead of data signal D and D\* as compared with drawing 6, and having received the output QPD of the phase-comparison part 40, and QPD\* instead of voltage controlled oscillator output VCO and VCO\*, the composition of latch circuitry is common. On the other hand, in the portion relevant to two pairs of FETQ<sub>51</sub>-Q<sub>52</sub> and Q<sub>53</sub>-Q<sub>54</sub> and outgoing ends equivalent to the NAND circuit of drawing 3, this circuit has original composition.

[0046]That is, each FET pair Q<sub>51</sub>-Q<sub>52</sub> and Q<sub>53</sub>-Q<sub>54</sub> receives the output of each latch circuitry in a gate, and it is constituted so that output PD of the phase-comparison part 10 and PD\* may validate selectively. Therefore, from the output of FET pair Q<sub>51</sub>-Q<sub>52</sub> and Q<sub>53</sub>-Q<sub>54</sub>, the complementary transform signal TR and TR\* are outputted mutually.

[0047]Drawing 8 is a figure in which making it put each other and showing the concrete example of composition of a part.

[0048]The three differential amplifiers 21, 22, and 23 with which this circuit was respectively constituted by one pair of FETQ<sub>61</sub> - Q<sub>66</sub> as shown in the figure, It comprises the current source part 81 constituted by FETQ<sub>67</sub> - Q<sub>69</sub>, respectively combining one pair of unit superposition parts X and Y which each comprised.

[0049]One output of the differential amplifier 22 is combined with the output of one way each of the differential amplifiers 21 and 23 in each unit superposition parts X and Y.

The output of another side of each differential amplifiers 21, 22, and 23 is also combined mutually.

Each differential amplifiers 21, 22, and 23 are connected to the current source 81 by FETQ<sub>67</sub> - Q<sub>69</sub>, respectively. each -- it is such -- composition -- having -- a unit -- superposition -- a part -- X -- Y -- mutual -- an output -- joining together -- having -- while -- further -- resistance -- R -- ' -- R -- -- zero -- -- ' -- a diode group -- D -- -- zero -- -- ' -- and -- FETQ -- -- zero -- -- ' -- constituting -- having had -- a reference voltage generating part -- G -- common -- connecting -- having -- \*\*\*\*

[0050]It was constituted as mentioned above, and piles up and output signal PD of the phase-comparison part 10 and PD\* are impressed to each gate of FETQ<sub>64</sub> and Q<sub>63</sub> which is one pair of inputs of the differential amplifier 22 in the unit superposition part X in a part. Output TR<sub>+</sub> of the converter 30 and TR<sub>+</sub>\* are impressed to the gate of FETQ<sub>61</sub> of the differential amplifier 21, and the gate of FETQ<sub>66</sub> of the differential amplifier 23, respectively. The reference voltage which the reference voltage generating part G generates is impressed to the gate of FETQ<sub>62</sub> of the differential amplifier 21, and FETQ<sub>65</sub> of the differential amplifier 23.

[0051]On the other hand, in the unit superposition part Y, output signal PD of the phase-comparison part 10 and PD\* are impressed to each gate of FETQ<sub>64</sub> and Q<sub>63</sub> which is one pair of inputs of the differential amplifier 22. Output TR<sub>-</sub> of the converter 60 and TR<sub>-</sub>\* are impressed to the gate of FETQ<sub>61</sub> of the differential amplifier 21, and the gate of FETQ<sub>66</sub> of the differential

amplifier 23, respectively. The reference voltage which the reference voltage generating part G generates is impressed to the gate of FETQ<sub>62</sub> of the differential amplifier 21, and FETQ<sub>65</sub> of the differential amplifier 23.

[0052]In the circuit constituted as mentioned above, that to which the sum of signal PD, PD\* and signal TR<sub>+</sub>, and TR<sub>+</sub>\* and the sum of signal PD, PD\* and signal TR<sub>-</sub>, and TR<sub>-</sub>\* were added further is outputted as the signal Q and Q\*.

[0053]In the reference voltage generating part G of the circuit shown in drawing 7 and drawing 8, as shown in a figure, When gate width of D<sub>0</sub> and FET is made into Q<sub>0</sub> for R<sub>0</sub>, R<sub>1</sub>, and the anode width of a diode, the resistance of resistance, Stable reference voltage can be generated to a temperature change and line voltage variation with easy composition Q<sub>0</sub>' and by producing so that D<sub>0</sub>' and R<sub>0</sub>' may satisfy the following formula 1 and the formula 2, respectively.

[0054]

[Formula 1]

$Q_0' = nQ_0$ ,  $D_0' = nD_0$ ,  $R_1' = (1/n) R_1$  [0055]

[Formula 2]  $R_0' - I_0' = R_0 - I_0 + R_0 I_1 / 2$

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## DESCRIPTION OF DRAWINGS

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[Brief Description of the Drawings]

[Drawing 1]It is a figure showing the fundamental composition of the phase frequency comparator circuit concerning this invention.

[Drawing 2]It is a figure for explaining the example of composition of a circuit and operation which can be used as the phase-comparison part 10 or 40 in the circuit shown in drawing 1.

[Drawing 3]It is a figure for explaining the composition and operation of a circuit which can be used as the converter 30 in the circuit shown in drawing 1.

[Drawing 4]It is a figure for explaining the composition and operation of a circuit which make repeat mutually in the circuit shown in drawing 1, and can be used as the part 20.

[Drawing 5]It is a figure showing the output signal of the phase frequency comparator circuit shown in drawing 1.

[Drawing 6]It is a figure showing the concrete example of composition of the circuit which can be used as a phase-comparison part.

[Drawing 7]It is a figure showing the concrete example of composition of the circuit which can be used as a converter.

[Drawing 8]It is a figure showing the concrete example of composition of the circuit which can be used noting that it piles up.

[Drawing 9]It is a figure showing the typical composition of the conventional phase frequency comparator circuit.

[Drawing 10]It is a figure for explaining the function of the phase-comparison part constituted using a D type flip-flop.

[Drawing 11]It is a figure showing the concrete example of composition of the phase-comparison part shown in drawing 10.

[Description of Notations]

10, 40 ... Phase-comparison part,

20 ... Superposition part,

30, 60 ... Converter,

50 ... Phase converter,  
21, 22, 23 ... Differential amplifier

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[Translation done.]